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LAUNCH SIGNAL RESPONDER
(UNITARY CONCEPT)
GENERAL DESIGN & OPERATION
CONCEPT

REPORT NO. LSE 154

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APPROVED BY

REVISIONS

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FORM NO. A-700-1

1.0 INTRODUCTION

The prime purpose of the Launch Signal Responder (LSR) is to check the proper operation of the Launch Control Logic Units and Control Panel. Other uses of the LSR may include exercising the Launch Control Logic Units between missile rotation periods and exercising the Launch crew.

The LSR permits the Logic Units & Launch Officer's Console to be operated as follows:

1. Simulated Countdown to Missile Away.

2. Simulated Countdown to Abort, Stop Commit & Return to Standby.

3. Simulated Countdown to Missile Ready & Return to Standby.

For the above operations the LSR will simulate all the ground support equipment (GSE) and missileborne equipment, however only to such an extent as to fullfill its prime purpose.

As far as the LSR fault location capability is concerned it has to be realized that a compromise had to be made between simplicity of procedure and complexity of equipment. The ultimate compromise of the present design of the LSR was to a major extent dictated by circumstances like already completely designed Logic Units and available space for components, rather than by free choice. The design was aimed towards a capability of locating faults to a sub-system level.

2.0 DEFINITIONS

2.1.0 Logic Unit

A master control device containing the necessary control circuitry to control the launching or abort sequences of all missile and all "GSE Sub-sytems".

2.2.0 Sub-System Sequencer

A functional division of the Launch Control Logic Units into sub-systems such as:

a. Pneumatic sub-system sequencer.

b. LO/2 sub-system sequencer.

2.2.1 End Component

A piece of GSE or missile equipment (outside the logic units) which controls a process upon receiving commands from the sub-system sequencer.

2.2.2 Process

A process is defined as a series of actions or changing conditions controlled by the end components such as:

a. Pressurizing

b. Filling with LO/2 or fuel

c. Activating a battery

d. Heating gyros.

2.3.0 Launch Signal Responder (LSR)

A device containing the necessary circuitry to check the operation of the Logic units.

2.3.1 Responder Sub-System

A functional breakdown of the LSR by sub-system analogous to the sub-system sequencers.

2.4.0 Major Command

An interface signal between sequencers in the Launch Control Logic Units.

2.0 DEFINITIONS (CONT'D

2.4.1 Major Incoming Command

A major command received by a sub-system sequencer.

[illegible]

2.4.2 Major Outgoing Command

A major command sent out by a sub-system sequencer.

2.5.0 Minor Command

A control signal to an end component in the missile or GSE.

2.6.0 Process Condition

A term which defines the status of the process such as:

a. LO/2 Tank Full.

b. Pressure Rising.

c. Doors Open Complete.

2.7.0 Response

A signal from an end component indicating a specific condition of the end component, or of a process condition.

2.8.0 LSR Interface Signal

An interface signal between LSR sub-system analogous to the major commands in the Logic units.

2.9.0 Sub-System Sequencer Step

A term describing a discrete change in one or more of the minor commands which will be maintained over a definite period of time.

2.9.1 Sub-System Sequencer Step Number

Steps will be numbered in time sequential order.

2.9.2 Sub-System Sequencer Step Name

The name of a process and whether it is being pre-conditioned, started, or stopped.

2.0 DEFINITIONS (CONT'D)

2.9.3 Internal Sub-Routine

A logic operation generated and used entirely within a sub-system sequencer to initiate a sub-system sequencer step.

2.10.0 Sub-System Matrix

A sub-system matrix is a rectangular arrangement of terms describing the position of the sub-system's end components (in vertical columns) at each sub-system sequencer step (Horizontal rows).

2.11.0 LSR Relay Matrix

LSR relay matrix is a sub-system matrix representing the end components position in terms of relay operation.

2.12.0 Sub-System Sequencer Status

A term describing one of the three phases of the launching sequence, or the abort sequence:

a. Standby

b. Countdown

c. Commit

d. Stop Commit

e. Return to Standby

2.13.0 Major Commands Routed Thru Sequencer

The above term refers to major incoming commands that are not used to initiate any change in a sub-system sequencer, but are changed in meaning (by the addition of a relay contact or contacts) and transmitted to another sub-system sequencer.

3.0 BASIC DESIGN PHILOSOPHY

3.1 System Black Box Presentation

The Launch Control System consisting of Launch Officer's Panel, Logic Units, Airborne & Ground Support Systems can be represented by "Black Boxes" on a sub-system basis as shown in figure 1.

In the responder check-out mode all connections of GSE and Airborne equipment (below line A-B of figure 1) are disconnected, and the LSR will receive the minor commands and generate the appropriate responses.

3.2 Sequencer Black Box Presentation

In figure 2 one particular sub-system sequencer is considered. Basically it generates the following categories of signals:

a. Minor Commands.

b. Major out going commands.

c. Signals for operating lights on the control panel.

It receives major incoming commands and responses from end components and process. The major incoming commands are the signals which will start the logic sequence of the sequencer; later on during the countdown cycle the responses may sometimes initiate such a sequence.

As a result of the logic sequence, the sequencer will generate its outgoing signals.

3.2.1 System Matrix

Keeping in mind that the main function of the Logic Unit is to operate the GSE and Airborne equipment correctly and in proper sequence, it will be clear that ultimately the minor commands are the main product of the Logic Units. Therefore a proper operation of the Logic Units means that the minor commands are generated correctly and in proper sequence during the countdown cycle.

In principle, therefore, a tabulation (Matrix) can be set up for the countdown cycle of the Logic Units, where horizontally the various minor commands are shown and vertically their change during the cycle will be indicated.
Since most of the minor commands are "go" or "no go" signals the nature of these commands can be shown by the presentation of Boolean Algebra, by respectively 1's and 0's.

3.0 BASIC DESIGN PHILOSOPHY

3.2.2 Sub System Matrix

The countdown cycle however, has a permissive progress and the sequencing progress of the various sub-systems in respect to each other may differ from case to case, and will also depend on the individual settings of certain time delay relays in each sequencer.

In the further consideration of the sub-system matrices the term "step" will be used for the horizontal rows. (See also definitions)

3.2.2.1 Major Commands and Matrix

The major commands generated by the sequencer are produced during a certain step or by a certain step plus an incoming major command, and can for that reason be related to respectively a certain step or a certain step plus major incoming command.

3.3 Basic LSR Check-out Concept

In view of the foregoing the basic LSR check-out concept will consist of:

a. Checking the minor commands against a pre-established sub-system matrix.

b. Checking that a step takes place by the correct initiating signal only.

c. Checking that the major commands are generated at the proper steps only.

The present design of the LSR does perform check (a) and (b) completely. Check (c) is only performed partially for reasons of simplicity of design as lined out in the introduction.

The major outgoing commands are checked only on the following points:

A. Command is not produced before generating step.
B. Command is produced at generating step.

No check is made on the presence or disappearance of a major outgoing command during steps following the generating step.

3.0 BASIC DESIGN PHILOSOPHY

3.4 Sub-System Isolation

In order to enable a fault location to a sub-system level, care had to be taken to isolate the various sub-system sequencers from each other to a certain extent. As the sequencers are connected by the major commands pre-cautions had to be taken to prevent feed back from the receiving to the sending sequencer. Where no isolation relays were available, the isolation was accomplished by inserting a diode at the receiving sequencer.

3.5 LSR Simulation

The sequencer sends minor commands to end components and receives ultimately responses back from GSE and Airborne Systems from end components or processes.

For this reason the responder has to contain a certain simulation part which simulates end components and processes.

The simulation has only to be a true one in so far as deviations from reality would reflect on the proper sequencer operation. In the present LSR design main events are executed in real time in order to obtain a countdown cycle in true time.

4.0 BASIC DESIGN CONCEPT

4.1 Minor Command Check

4.1.1 Responder Matrix

The end components are simulated in the LSR by relays, the minor commands relays K1 thru Kn in figure 3, which will receive the commands generated by the sequencer. At a certain step the sequencer is supposed to send out a specific combination of minor commands only. Thus certain minor command relays will be energized, certain other ones will be de-energized.

So for each step of the sub-system matrix, a corresponding status of relays K1 thru Kn can be shown, which if arranged in a tabulated form will result in another matrix: The Responder Matrix.

4.0 BASIC DESIGN CONCEPT

4.1.2 Relay Tree

In order to check on the proper minor command combination for a step, an individual series combination of contacts of relays K1 thru Kn can be made for each step and checked for continuity. In figure 3 continuity will show a voltage at one of the points 1 thru n.

In figure 3 for each step the relay conditions are shown by separate contacts. It is obvious that certain steps will have certain same relay conditions in common, or even certain same combinations of relay conditions.

Therefore by combining these a type of relay tree can be developed, which will employ a minimum number of contacts. In other words the responder matrix can be developed into an optimum relay tree. During the design an empirical way was obtained for optimizing larger matrices, a discussion of which however is beyond the scope of this report. A typical tree is shown in figure 4.

4.1.3 Minor Command Fault Check

The function of the responder is to check that voltage at the tree branches 1, 2, 3, etc. of figure 4 appears correctly, continuously and in correct sequence. For this purpose a telephone type stepping switching is used in an arrangement shown in figure 5.

The present command wafer checks on the continuity of a minor command combination by means of a minor command fault relay, a time delay relay, which drops out if the voltage disappears for a period exceeding 500 milli-seconds.

The advance command wafer takes care of the stepping procedure of the switch.

Suppose the sequencer is in step 3 of its cycle. In that case the wiper will be in position 3. The minor command fault relay checks on the continuity of voltage from branch 3 of the relay tree.

Suppose now the sequencer cycles to step 4. The voltage of branch 3 disappear, and will appear at 4.

4.0 BASIC DESIGN CONCEPT

4.1.3(Cont) Since point 4 of the tree is wired to position 3 of the advance command wafer and the stepping switch is still in position 3, the advance command relay will pick up, energizing the switch stepping relay, ultimately resulting in a step of the switch.

The minor command fault relay, which due to its time delay, remains picked up during the stepping period, will now be connected to point 4 of the present command wafer and will again receive voltage but now from point 4 of the tree.

If a minor command combination appears out of sequence, the stepping switch will not advance and the minor command fault relay will drop out after 500 milli-seconds.

4.2 Major Outgoing Command Check

A major command generated in the sequencer will energize a major outgoing command relay in the responder, see figure 6.

The check on these commands are made with the same stepping switch as used for the minor commands. As mentioned under 3.2.2.1 a major outgoing command will be related to a certain step. The present design checks that the command does not appear before this step by means of the "too early" wafer and that it is generated at the proper step by the "too late" wafer.

As shown in figure 6 a fault will appear as energizing of the "outgoing command not OK" relay.

As mentioned under 3.3 the duration of a major outgoing command over a certain number of steps is not checked.

4.3 Responder Indications

Three major means are provided to indicate the situation during the responder check-out mode:

a. The position of the stepping switch is indicated by a pulse counter, which will show which steps the sequencer has completed.
b. All major incoming commands are displayed by a green light.

4.0 BASIC DESIGN CONCEPT

4.3 (Cont) c. A responder sub-system status light, which shows:

1. Green if a phase of the countdown is completed by the sequencer.
2. No display if a phase of the countdown is in progress.
3. Red if either the minor command fault relay drops out or one of the major outgoing commands fault relays picks up.

The green indication of the status light is operated from the status wafer of the stepping switch.

The red indication is operated indirectly from the individual fault relays, as these are monitored by the so called "Stop Relay", which locks itself in. (See figure 7)

4.4 Homing of Responder to Zero Position

The responder will come back to its zero position if the stepping switch steps back to its zero position.

The return to zero of the stepping switch is accomplished by the homing wafer of the stepping switch itself.

Homing will automatically take place if the responder system power has been turned off and is turned on again.

In that case the homing relay has dropped out and will not pick up before the stepping switch has returned to zero. (Refer to figure 8). The dropped out homing relay connects the homing wafer to the advance command relay which will result in a stepping of the stepping switch to its zero position.

4.5 Fault Insertion

Switches are inserted in certain responses of the responder, which will allow the simulation of faults in GSE or Missile equipment.

They can be used either for additional checks on the sequencer or for training purposes.

4.6 LSR Sys-system Test

The design has made provisions to make a limited test on the operation of the responder sub-system.

4.0 BASIC DESIGN CONCEPT

4.6 (cont) Each responder sub-system is tested individually while disconnected from the sequencer. The test is made normally by procedure. For this purpose a separate telephone type stepping switch is provided for each responder sub-system, which is advanced by a manually operated push button (figure 9, stepping advance). The position of this stepping switch is indicated by a pulse counter, the test counter. At each step the stepping switch will generate all incoming signals for the responder, consisting of:

a. The minor commands, which will be programmed in correppondence with the responder matrix.

b. Major incoming commands, programmed in proper relation to the responder matrix.

c. Major outgoing commands, programmed also in proper relation to the responder matrix.

Consequently the responder stepping switch will follow the test stepping switch. Visual comparison of the system counter and the test counter and the absence of the red status light indication shows proper operation of the major part of the responder.

The test stepping switch and the test counter is reset to zero by a special reset button. (Figure 9, manual reset).

In order to test the major outgoing command fault relays a major outgoing command test switch is provided. By actuating this switch, during a particular step, the simulated outgoing commands are interrupted and after 500 milli-seconds the relay will pull in, and the status light goes red.

A stop reset button is provided to release the stop relay again during the test in order to be able to advance the stepping switches to the subsequent steps.

a. During the stepping of the Test Stepping Switch, the power from the simulation wafers to the various command relays is interrupted by the Test Power Lockout Relay in order not to exceed the current breaking capacity of the stepping switch contacts.

4.7 Responder Interface signals

Some sequencers receive responses from processes controlled by other sequencers. In order to obtain the same effect in the responder checkout mode, in such cases a signal is required between the related responders, which is defined as a responder interface signal.

4.0 BASIC DESIGN CONCEPT

4.8 Deviating Responder Sub-System Design

All but two responder sub-systems are built up from the previous described basic elements.

Excepted are:
a. The countdown sub-system responder.
b. The propellant level sub-system responder.

The basic reason for this deviation is that both sequencers deviate from all other sequencers in that they do not generate minor commands, since they do not operate end components. Both systems produce only major outgoing commands, which are generated by either major incoming commands or process responses, and do not have a pre-established sequence.

Therefore both the countdown and the propellant level responders do not have a responder stepping switch.

The countdown sub-system responder is kept in the most simple possible form and consists of manually operated switches, simulating incoming commands, and indication lights showing proper generation of outgoing commands. This responder does not participate in the Automatic Responder test, but will allow a manual check prior to such an automatic test, according to a written procedure. In the propellant level responder, only a major outgoing command check is made. This responder has a normal simulation part.

The countdown responder does not have a sub-system test feature. The propellant level responder has a test stepping switch which performs a gross check on the proper operation of the relays.

5.0 RESPONDER CHECKOUT MODE PROCEDURE

5.1 Preparations for Checkouts

All ground and airborne systems are assumed to be in tactical mode and in standby condition.

Then the following steps have to be taken to go over into a responder mode:

a. Transfer the missile pressurization from the pneumatic sub-system to an auxiliary pressurization unit, since the responder mode operation will interfere with the normal standby pressurization.

5.0 RESPONDER CHECKOUT MODE PROCEDURE

5.1 (cont'd)

b. Turn off sub-system power on all sequencers except Re-entry Vehicle and Guidance.

c. Switch cables connecting the logic units with the umbilical junction box at the junction box end from the "Standby Mode" to the "Responder Checkout Mode" connections. (This does not apply to Re-entry Vehicle and Guidance).

d. Switch transfer switches in the bottom sections of the responder units from "Standby" to "Responder" mode.

e. Obtain "Launch Enable" signal from Squadron Command Post.

5.2 Countdown Sequencer Pre-check

Upon completion of steps (a) thru (e) of 5.1 the logic and responder units are ready for a responder checkout operation. The first part of this will consist of a manual check of the countdown system since this responder as explained before does not participate in the automatic checkout procedure. For this check the sub-system power has to be turned on at the countdown responder.

Check the sequencer according to a written procedure. The check will consist of operating manually switches in a certain sequence and by observing the indication of certain lights on the front panel of the countdown responder chassis and Launch Officer's console. Upon successful completion of the test put all switches again in their off position and turn off the responder power.

5.3 Automatic Checkout Start

To start the automatic checkout the following steps have to be taken:

a. Turn on responder sub-system power on all responders.
b. Turn on sequencer sub-system power on all sequencers.

All sub-systems should now obtain their "Standby" condition, resulting in green standby lights on the Launch Officers Control Panel. This green display for some sub-systems will be reached via a red one first, which will set off the alarm and require the actuation of the reset button on the control panel. All responder status lights shall display green. Each responder system counter shall indicate the number corresponding with the sub-systems final step number for "Standby".

5.0 RESPONDER CHECKOUT MODE PROCEDURE

5.4 Simulated Countdown

The simulated countdown can be started after completion of 5.3 and is initiated in the same way as a real countdown, by acthating the "Start Countdown" button on the officer's control panel.

If all systems operate prpperly, the status lights will progress to"ready"and "Missile Ready" will appear.

All responder status lights, which at the start of the countdown cycle lost their display, shall show green again.

Each system counter will display a pre-established number for each sub-system.

In a similar way the "Commit" cycle can be completed, and will be initiated also from the control panel.

The responder design also permits a "Return to Stan dby" and a "Stop Commit" cycle, but only from respectively the "Missile Ready" and the "Abort" status.

5.5 Re-Setting the Responder Mode Operation to Zero

In order to reset a once started or completed responder checkout operation to its zero position, the following steps have to be taken:

a. Turn off all sequencer sub-system power
b. Turn off all responder sub-system power

The logic and responder units are now ready again for a responder mode checkout start as described under 5.3.

The responder system stepping switch remains in its last or ultimate position after the power has been turned off, however, as described before, it will return to zero position as soon as the power is turned on again.

6.0 FAULT LOCATION PROCEDURE

6.1 General Concept

In case any of the sequencers faults during the responder checkout mode, one or some of the status lights will not come on green and some may turn red. By a procedural check of those sub-systems which do not have a green status light, the system which is at fault can be determined.

6.2 Major Command Matrix

One of the tools required to determine which sub-system is at fault is a major command matrix.

This matrix will have to present horizontally all the major commands received and generated by the sub-system sequencer under consideration and should indicate by which sequencer an incoming command is generated.

The vertical column should show the incoming commands required for each sequencer step and the outgoing commands generated by the step.

Using the Boolean Algebra notation for this matrix, the required presence of an incoming command or the generating of an outgoing one can be presented by 1's, the required absence of an incoming or no generation of an outgoing command by 0's and no requirement for an incoming command by a blank space.

6.3 Fault Indication

If during a particular cycle of the responder mode operation all responder status lights become green, all sub-systems have performed this cycle satisfactorily.

If one or more green indications are missing, after elapse of a pre-established period of time, or one or more sub-systems show a red status light this means definitely that the cycle was not performed satisfactorily.

6.0 FAULT LOCATION PROCEDURE

6.4 Fault Location

The responder-provided tools for detecting the faulty sub-system are the status light, the system counter, the major incoming command lights and the major command matrix.

For the sub-systems not showing a green responder status light, the counter reading and the major incoming commands that have been received (indicated by lights) are compared with the major command matrix.

The following cases can be distinguished:

a. Counter reading agrees with the major incoming COMMANDS COMBINATION.

   1. No status light display indicates sequencer is alright but, did not continue due to lack of further required major incoming commands.

   2. Red status light, indicates sequencer is at fault.

b. Counter reading disagrees with major incoming commands combination.

   In this case first the correctness of the disagreeing incoming commands has to be checked, by going back to the generating sub-systems and comparing it with their matrix and counter reading. Depending on whether the generating systems are satisfactory or at fault it can be concluded whether the original sequencer is correspondingly at fault or alright.

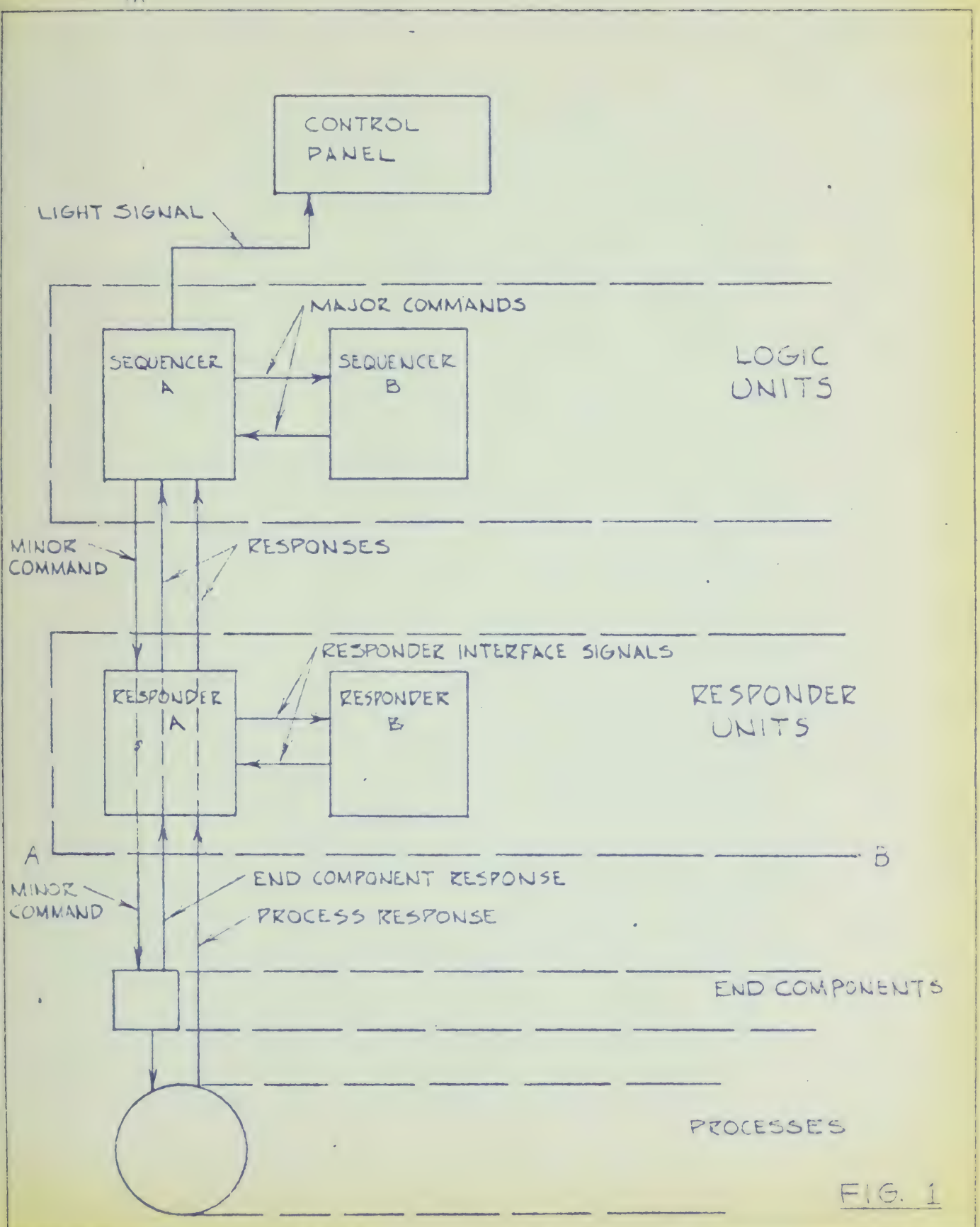

CONTROL PANEL
LIGHT SIGNAL
MAJOR COMMANDS
SEQUENCER A
SEQUENCER B
LOGIC UNITS
MINOR COMMAND
RESPONSES
RESPONDER INTERFACE SIGNALS
RESPONDER A
RESPONDER B
RESPONDER UNITS
A
B
MINOR COMMAND
END COMPONENT RESPONSE
PROCESS RESPONSE
END COMPONENTS
PROCESSES

FIG. 1

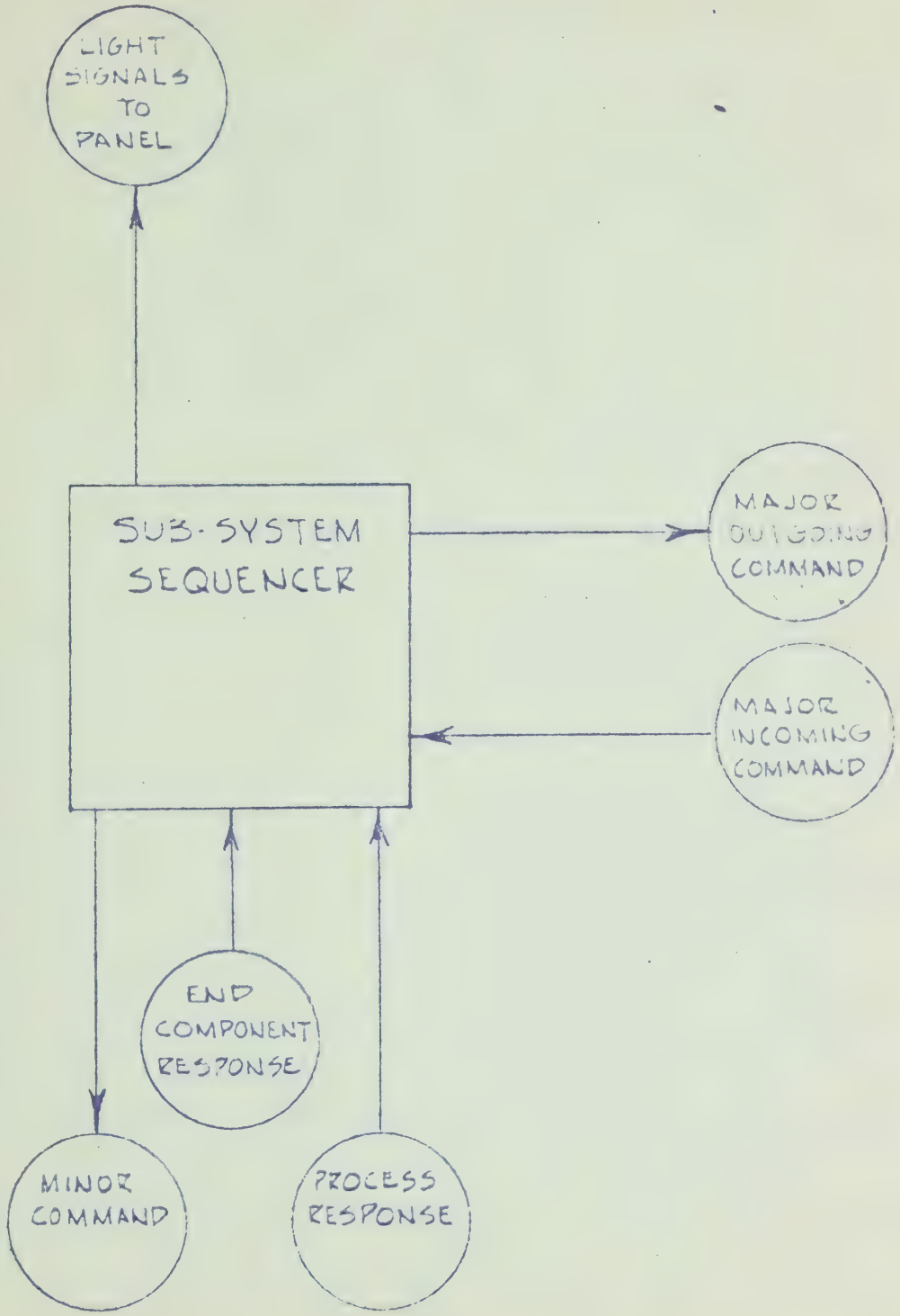

LIGHT SIGNALS TO PANEL
SUB-SYSTEM SEQUENCER
MAJOR OUTGOING COMMAND
MAJOR INCOMING COMMAND
END COMPONENT RESPONSE
MINOR COMMAND
PROCESS RESPONSE

FIG. 2

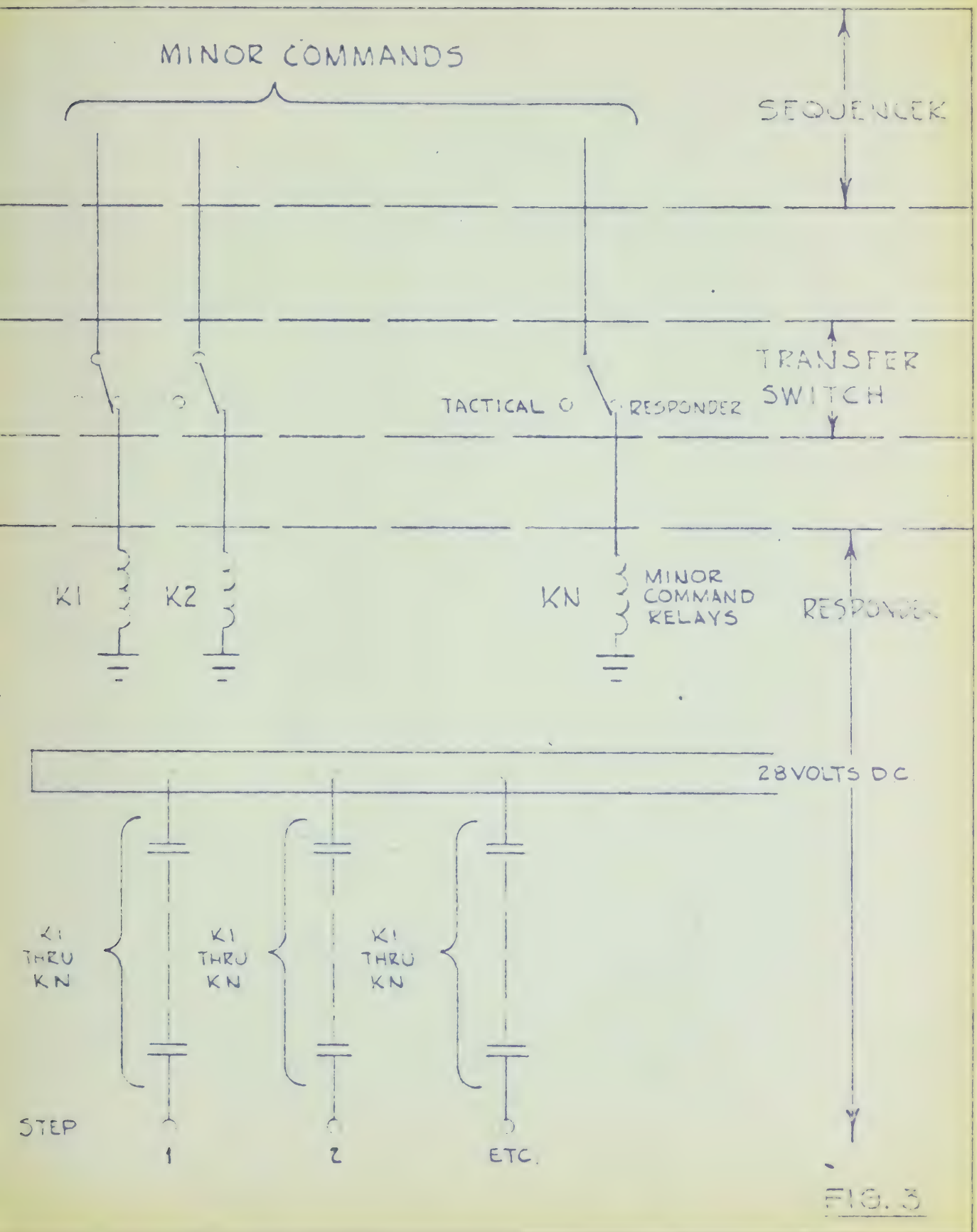

MINOR COMMANDS
SEQUENCER
TRANSFER SWITCH
TACTICAL
RESPONDER
K1
K2
KN
MINOR COMMAND RELAYS
RESPONDER
28 VOLTS DC
K1 THRU KN
K1 THRU KN
K1 THRU KN
STEP
1
2
ETC.

FIG. 3

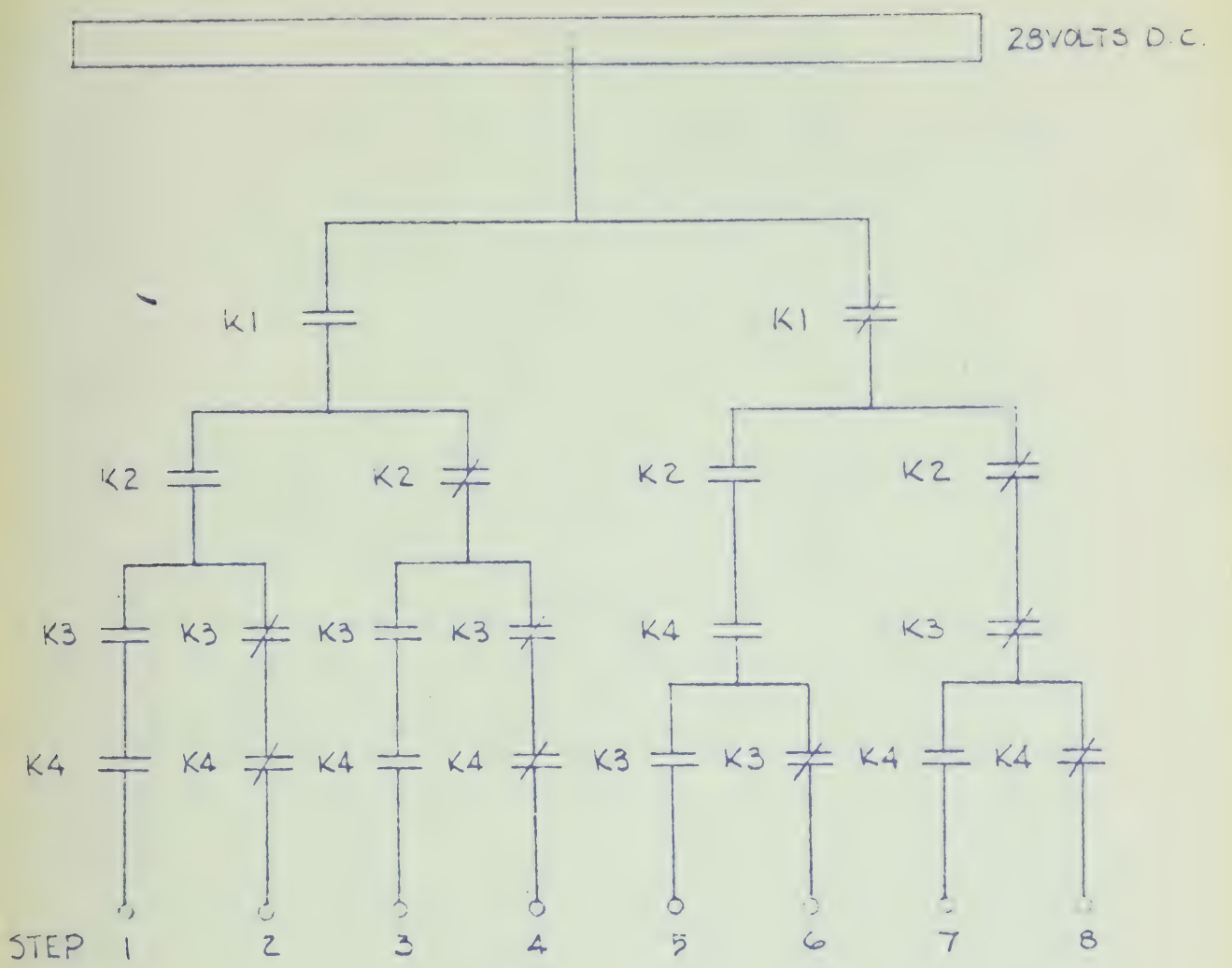

28VOLTS D.C.
K1
K1
K2
K2
K2
K2
K3
K3
K3
K3
K4
K3
K4
K4
K4
K4
K3
K3
K4
K4
STEP 1
2
3
4
5
6
7
8

FIG. 4

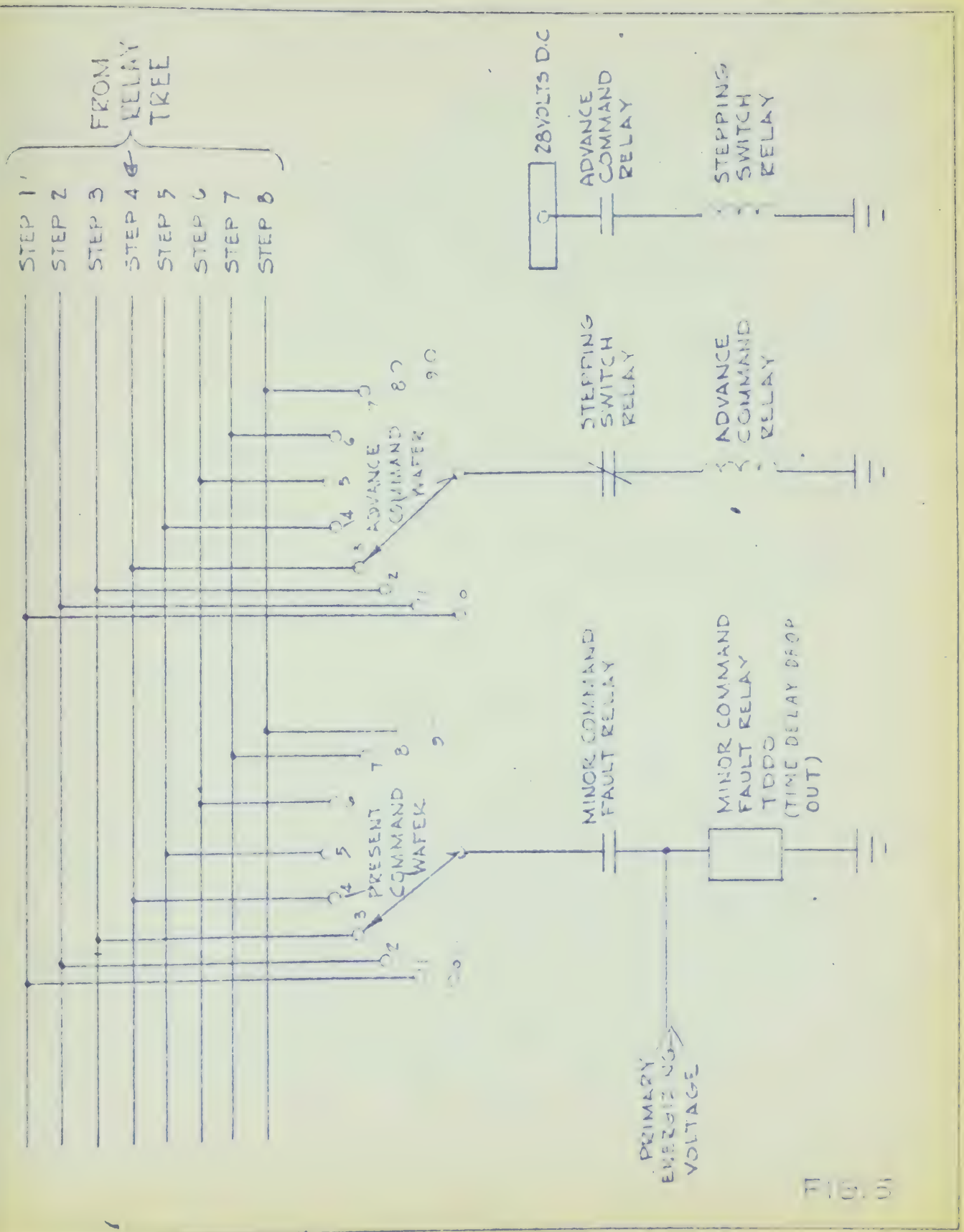

FROM RELAY TREE
STEP 1
STEP 2
STEP 3
STEP 4
STEP 5
STEP 6
STEP 7
STEP 8
28 VOLTS D.C
ADVANCE COMMAND RELAY
STEPPING SWITCH RELAY
STEPPING SWITCH RELAY
ADVANCE COMMAND RELAY
ADVANCE COMMAND WAFER
MINOR COMMAND FAULT RELAY
MINOR COMMAND FAULT RELAY TDDO (TIME DELAY DROP OUT)
PRESENT COMMAND WAFER
PRIMARY ENERGIZE VOLTAGE

FIG. 6

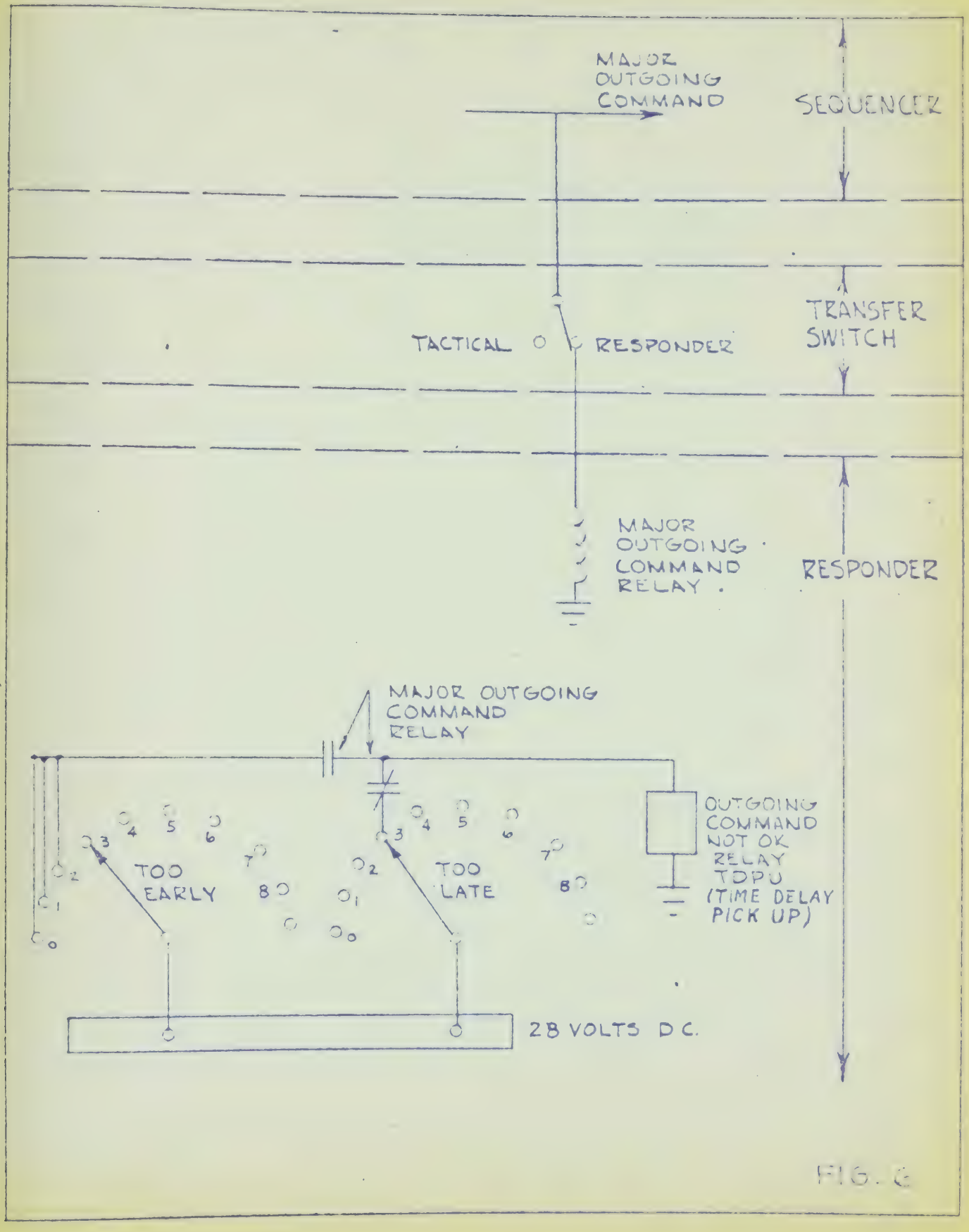

MAJOR OUTGOING COMMAND
SEQUENCER
TRANSFER SWITCH
TACTICAL
RESPONDER
MAJOR OUTGOING COMMAND RELAY
RESPONDER
MAJOR OUTGOING COMMAND RELAY
TOO EARLY
TOO LATE
OUTGOING COMMAND NOT OK RELAY TDPU (TIME DELAY PICK UP)
28 VOLTS D.C.

FIG. 6

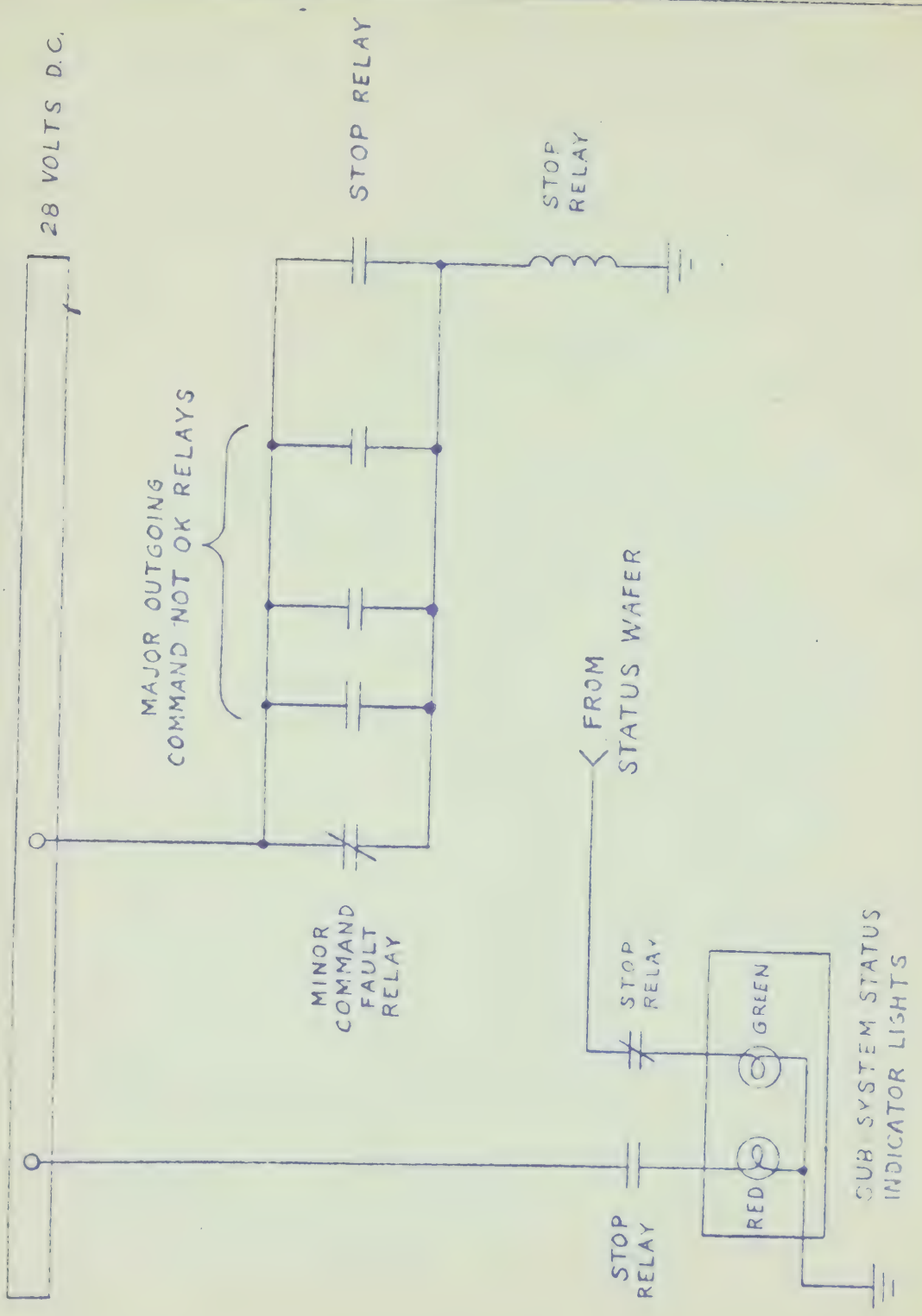

28 VOLTS D.C.
STOP RELAY
STOP RELAY
MAJOR OUTGOING COMMAND NOT OK RELAYS
FROM STATUS WAFER
MINOR COMMAND FAULT RELAY
STOP RELAY
GREEN
RED
SUB SYSTEM STATUS INDICATOR LIGHTS
STOP RELAY

FIG. 7

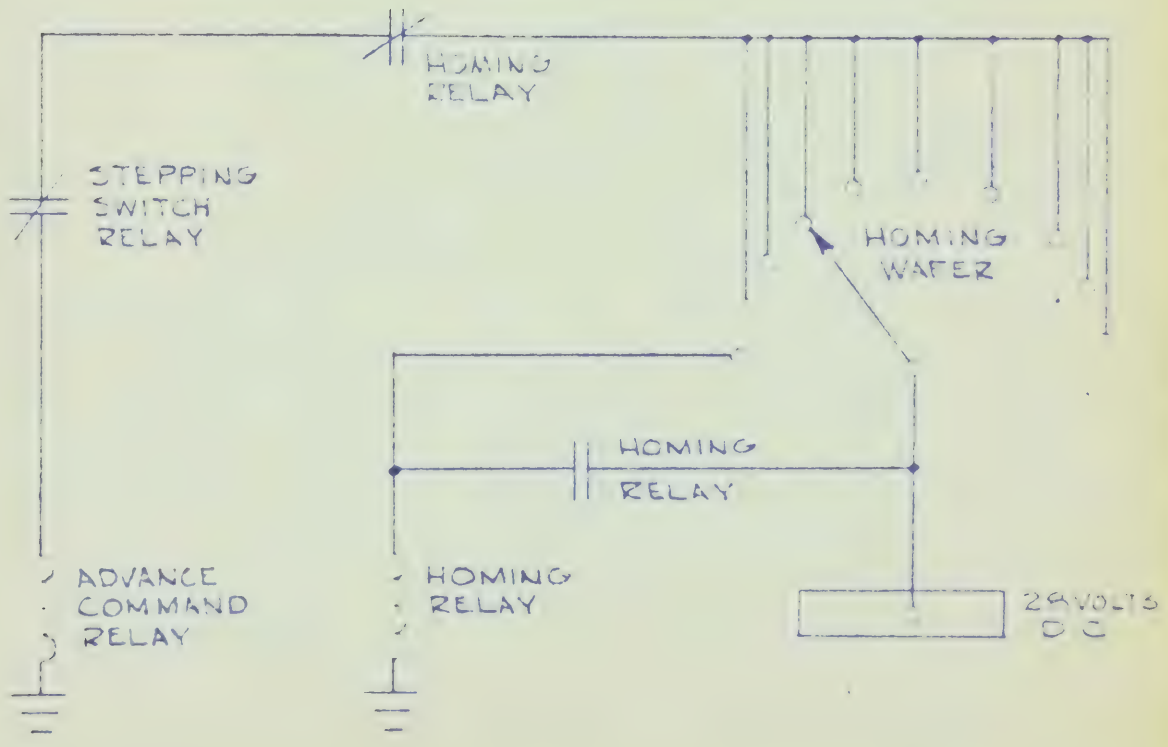

HOMING
RELAY
STEPPING
SWITCH
RELAY
HOMING
WAFER
HOMING
RELAY
ADVANCE
COMMAND
RELAY
HOMING
RELAY
28 VOLTS
D C

FIG 3

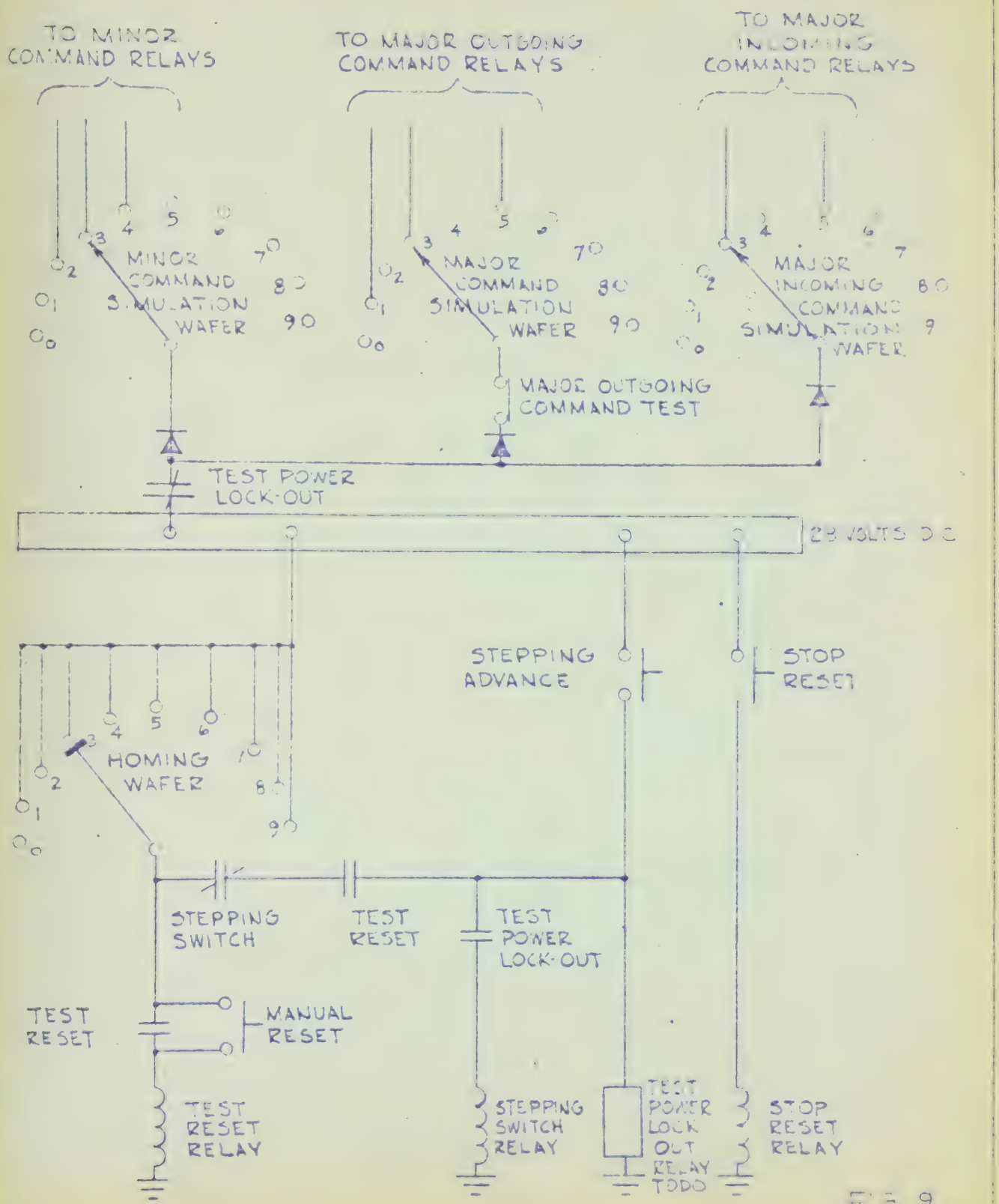

TO MINOR COMMAND RELAYS
TO MAJOR OUTGOING COMMAND RELAYS
TO MAJOR INCOMING COMMAND RELAYS
MINOR COMMAND SIMULATION WAFER
MAJOR COMMAND SIMULATION WAFER
MAJOR INCOMING COMMAND SIMULATION WAFER
MAJOR OUTGOING COMMAND TEST
TEST POWER LOCK-OUT
28 VOLTS D C
HOMING WAFER
STEPPING ADVANCE
STOP RESET
STEPPING SWITCH
TEST RESET
TEST POWER LOCK-OUT
TEST RESET
MANUAL RESET
TEST RESET RELAY
STEPPING SWITCH RELAY
TEST POWER LOCK OUT RELAY TODO
STOP RESET RELAY

FIG. 9

INDEX

1.0 INTRODUCTION

1.1 Scope and Purpose

This design criteria is written to define and establish the basic design philosophy of the Launch Signal Responder, (LSR).

This design criteria will outline and define the complete design task of the LSR based on the premise of minimum change in the presently designed Launch Control System.

A general example outlines a complete step by step design of a typical LSR subsystem. For better understanding of the interface problem between the sequencer subsystem and the LSR Subsystem the Logic Unit Sequencer design is included in the design example.

1.1.1 Overall System Description

The LSR in the Responder mode will exercise the Launch Control System in real time, and isolate malfunctions to a particular subsystem in the Logic Unit. The LSR will also have an automatic test capability on the subsystem level.

2.0 GENERAL DESCRIPTION OF LSR

2.1 Basic Design Concept

The basic design concept of the LSR is based on checking that the output of the Logic Unit Sequencers corresponds to a definite pre-established operational sequence of the end components which are controlled by the Logic Unit Sequencers.

This is accomplished by checking the outputs of the sequencers to a pre-established fixed control matrix.

The interface signals between subsystem sequencers will be checked with respect to their relative position in the sequence.

The process of a definite operational sequence of the end components is simulated in the LSR.

Monitoring of the simulated process in the LSR will establish the physical relationship between the various subsystems.

Checking the intermediate steps of the process in the LSR with the acknowledgments received from the sequencers determines whether the sequencer responses are true or false.

3.0 DEFINITIONS FOR DESIGN PHILOSOPHY AND CRITERIA

3.1 Definitions

In order to establish a uniform design for the LSR the terms used in the design philosophy are defined below:

3.1.1 Definition of Command

Command is defined as a control signal which will initiate a change in the sequence of operation.

3.1.1.2 Definition of Major Command

A major command is defined as an interface signal between sequencers

3.1.1.2.1 Definition of Major Incoming Command

A major incoming command is defined as a control signal received by the sequencer to initiate a logic sequence in the subsystem.

3.1.1.2.2 Definition of Major Outgoing Command

A major outgoing command is defined as a control signal sent by the sequencer to start a logic sequence in the subsystem receiving the signal.

3.1.1.3 Display of Commands

3.1.1.3.1 Major Incoming Command Display

All major incoming commands will be displayed on the LSR subsystem panel by a green light.

3.1.1.3.2 Display of Major Outgoing Commands

No major outgoing command will be individually displayed on the LSR - subsystem panel.

If an outgoing command does not appear or is out of sequence the LSR subsystem status light will indicate a red condition and the LSR sequence will stop.

3.1.1.3.2 Display of Major Outgoing Commands - cont.

For general conditions circuit will be as in design example. If an outgoing command does not appear in the tree a priority check on the incoming command is made.

3.1.1.4 Definition of Minor Command

A minor command is defined as a control signal to any end component in the missile or GSE for any phase of operation.

3.1.1.5 Minor Command Display

No individual minor commands will be displayed on the LSR Subsystem panel. Indication in form of a numerical display will be provided to indicate the number of a minor command being generated by the Logic Unit Sequencer.

If a minor command does not appear or is out of sequence the LSR Subsystem Status Light will indicate a malfunction.

When a Subsystem sequence is completed satisfactorily the LSR Subsystem Status Light will become Green, indicating satisfactorily Subsystem operation.

3.2 System for Matrix Representation

The following conditions are established to standardize system design.

3.2.1 Valve Command Representation

3.2.1.1 Motor Operated Valves

The motor operated valve will be represented by a latching relay consisting of Coil A and Coil B.

In Valve Matrix (Open Valve Position = 1
(Closed Valve Position = 0

In Relay Matrix (Energized Contact of Coil A = X
(Energized Contact of Coil B = X'

X' = 0 X = 0

3.2.1.2 Pneumatic or Solenoid Operated Valves

The pneumatic or solenoid operated valves will be represented by a normal relay.

In Valve Matrix (Open Valve = 1
(Closed Valve = 0

In Relay Matrix (Energized Relay Contact = Y
(Deenergized Relay Contact = Y'

then in relay matrix Y = 1
Y' = 0

Note: For normally closed valves valve matrix terms equal relay matrix terms. For normally open valves the valve matrix terms are opposite to the relay matrix terms.

3.2.2 End Components Representation

Accomplishment of a positive action which requires application of power such as activate battery, missile loads on, etc., will be designated as 1.

Reverse condition as 0.

3.3 Fault Insertion

General Fault Insertion -

The Faults are inserted in the feedback or replay circuit of the end components or in the control circuitry depending on individual case.

3.3.1 Individual Fault Insertion

a. For end components there will be limited Fault Insertion.

b. Major Incoming Commands partial Fault Insertion.

(Command failed to appear)

c. Major Process Parameters.

d. Partial Fault Insertion.

3.4 Design Philosophy

For the proper operation of the LSR a specific procedure has to be followed prior to exercising the Launch Control System in the Responder mode. The same procedure has to be followed in case a malfunction has appeared in one or more sequencers during the Responder Mode.

3.4.1 Resetting the LSR

Resumption of Launch Control System checkout through the LSR after an occurrence of a malfunction will be accomplished as follows:

a. All power is shut off in each Logic Unit Sequencer.

b. All power is shut off in each LSR Subsystem.

Upon replacement of faulty sequencer in the Logic Unit power is turned on in the LSR and Logic Units. When no malfunction occurs and standby condition is established for all Logic Unit Sequencers a responder countdown and check is initiated.

3.4.2 Major Commands in Series Interface Between Sequencers.

When there is a series chain of outgoing major commands in various Logic Unit Sequencers a special arrangement is made in each Logic Unit Sequencer.

Two possibilities exist to achieve the desired results. They are presented in order of simplicity.

a. Arrange contacts in sequential order versus time. 28 V is applied at the first command.

b. Insertion of an isolation relay in the sequencers which are in the middle position of the series string.

c. Isolation between Logic Unit Sequencers will be accomplished by inserting a diode at the receiving Logic Unit subsystem.

Note: See design example sequencer sketch.

3.4.2 Major Commands in Series Interface Between Sequencers

d. Any major incoming command which forms a series string through the Logic Unit sequencer will not be displayed on the LSR subsystem panel.

Note: Diode isolation will be provided in the receiving logic unit subsystem. A relay in the LSR will indicate the presence or absence of the above defined command.

4.0 TYPICAL DESIGN EXAMPLE

4.1 Description of Physical Process

The objective is to load the upper tank with fluid in two phases of operation.

Upon load completion a line drain is desired.

Valve matrix in effect Fig. will explain the process completely.

4.1.1 Problem

The problem consists of designing an LSR to the existing sequencer that will fulfill the requirements outlined in this criteria.

5.0 LSR SUBSYSTEM TEST

5.1 LSR Subsystem Test Criteria

The LSR subsystem test is performed to obtain assurance that the LSR subsystem indicating a malfunction in the Logic Unit sequencer is functioning properly.

5.1.1 Design Philosophy of the LSR Subsystem Test

The design objective of the LSR subsystem test is to determine in minimum time the integrity of the LSR sequence. This is accomplished by simulating all incoming and outgoing signals into the LSR subsystem.

5.1.2 LSR Subsystem Test Procedure

The LSR subsystem test is performed as follows:

a. Panel power is shut off in the corresponding Logic Unit subsystem.

b. LSR load test is placed in test position.

5.1.2.1 Major Incoming Command Test

a. Set responder switch at launch mode and unplug the LSR plugs at the umbilical junction box.

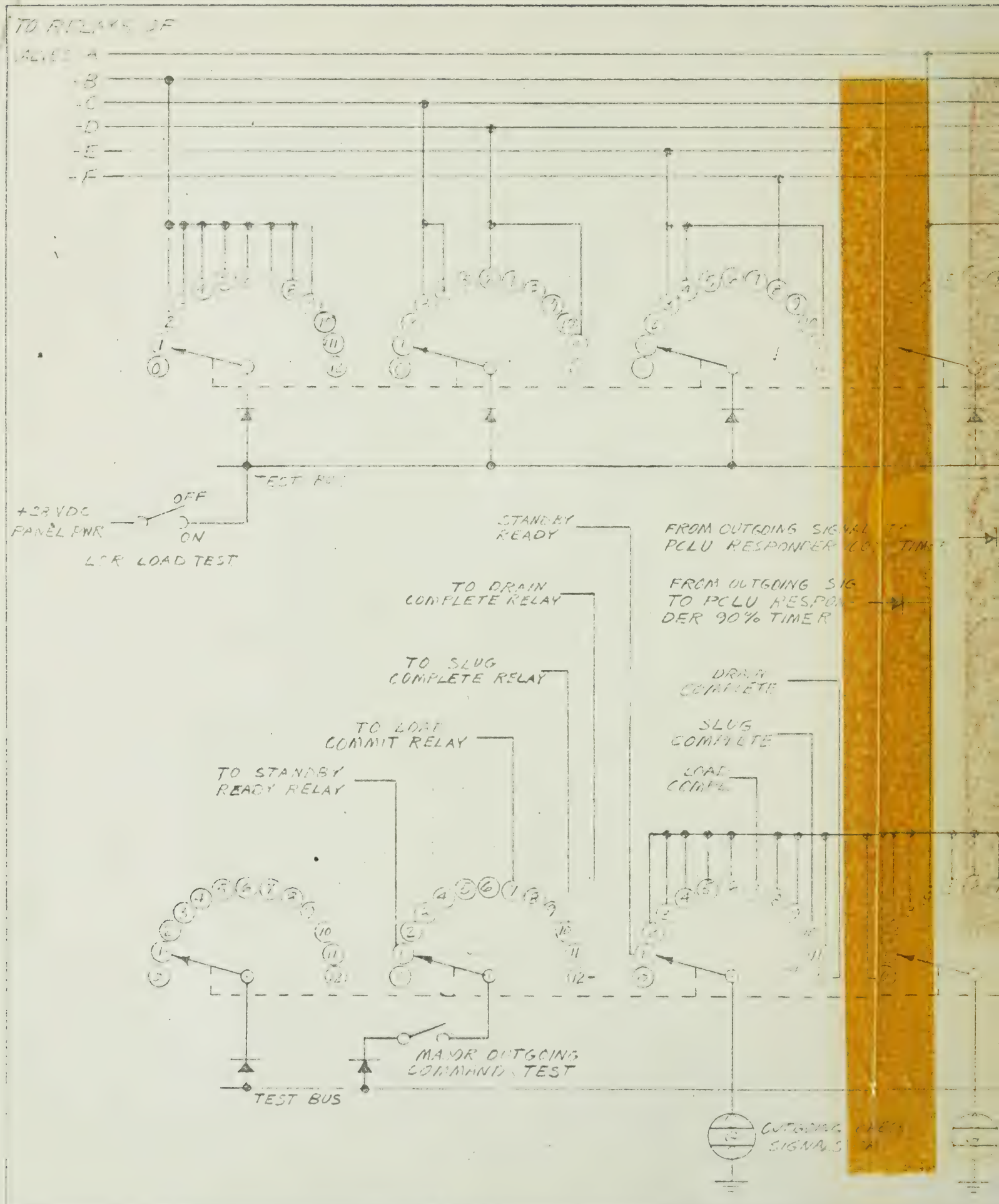
b. Major incoming command test switch is placed in test position and all major incoming command lights will illuminate (green). Nondisplayed major incoming command test light will illuminate (green).

5.1.2.2 LSR Subsystem Sequence Test

The LSR subsystem sequence test will be performed by a stepping switch. The stepping switch will be advanced manually and a visual comparison between two counters is made by the operator. Corresponding numbers on the numerical displays will indicate a "Go" condition and then the next step shall be performed.

5.0 SUMMARY

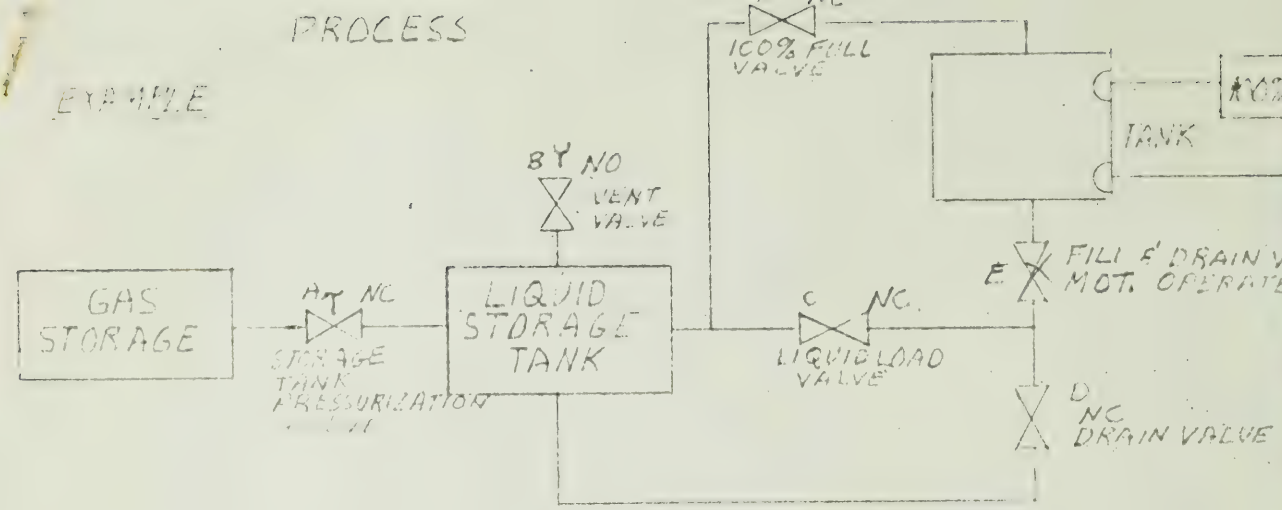
This design criteria and circuitry developed in the example LSR design will be used throughout the design of the LSR for the existing Launch Control System of EOC concept.


TO RELAYS OF
A
B
C
D
E
F
+28 VDC
PANEL PWR
OFF
ON
LCR LOAD TEST
STANDBY
READY
TO DRAIN
COMPLETE RELAY
TO SLUG
COMPLETE RELAY
TO LOAD
COMMIT RELAY
TO STANDBY
READY RELAY
FROM OUTGOING SIG
TO PCLU RESPON-
DER 90% TIMER
DRAIN
COMPLETE
SLUG
COMPLETE
LOAD
COMPL
MAJOR OUTGOING
COMMAND TEST
TEST BUS

COUNTDOWN SEQUENCE
SLUG LOAD COMPLETE
+28V
SLUG LOAD COMP
LSR
DRAIN COMP
RETURN TO STANDBY
STANDBY READY
COMMIT
DRAIN RELAY
CLOSED
DRAIN COMPLETE
NOT
DRAIN
28V STANDBY
LOAD RELAY
NOT 100% FULL
COMMIT RELAY
NOT OPEN
OPEN
LIQUID STORAGE PRESSURE NOT LOW
LIQUID SUPPLY OK
MANUAL VALVES READY
AUTO. VALVES READY
5" VALVE CLOSED
VALVES

PROCESS

EXAMPLE



1 = OPEN 0 = CLOSED

STEP I SETUP VALVE MATRIX

		A	B	C	D	E	F
1	MAJOR COMMAND STANDBY	1	0	1	1	1	1
2	MAJ. COM. START COUNTDOWN	1	1	1	1	1	1
3	MIN. COM. START	1	1	0	1	0	1
4	MIN. COM. START	1	1	0	0	1	1
5	MAJ. COM. 90% FULL	1	1	1	1	1	1
6	MIN. COM. START	1	1	1	0	1	1
7	MIN. COM. START	1	1	1	1	1	1
8	MAJ. COM. COMMIT	1	1	1	1	1	0
9	MAJ. COM. 100% FULL	1	1	1	1	1	1
10	MIN. COM. #5	1	0	1	1	1	1
11	RETURN TO STANDBY FROM END OF COUNTDOWN	1	0	1	0	0	1
12	MIN. COM. #6 DRAIN COMPLETE	1	0	1	1	1	1

STEP II DRAW RELAY MATRIX

	A	B	C	D	E	F
1	1	1	1	1	1	1
2	1	0	1	1	1	1
3	1	0	0	1	0	1
4	0	0	0	1	0	1
5	1	0	1	1	1	1
6	1	0	1	0	1	1
7	1	0	1	1	1	1
8	0	1	1	1	1	0
9	1	0	1	1	1	1
10	1	1	1	1	1	1
11	1	1	1	0	0	1
12	1	1	1	1	1	1

STEP III SOLVING OF RELAY MATRIX

a. REDUCE THE MATRIX BY REMOVING ROWS IN WHICH CONTACTS ARE DUPLICATED

	A	B	C	D	E	F
1	1	1	1	1	1	1
2	1	0	1	1	1	1
3	1	0	0	1	0	1
4	0	0	0	1	0	1
6	1	0	1	0	1	1
8	0	0	1	1	1	0
11	1	1	1	0	0	1
# OF "1"	5	2	5	5	4	6
# OF "0"	2	5	2	2	3	1

b. OPTIMIZE FOR MINIMUM CONTACT COMBINATION TAKE OUT E DEVELOPE SUB MATRIX OVER B COLUMN

E

	A	B	C	D	F
3	1	0	0	1	1
4	0	0	0	1	1
11	1	1	1	0	1

c. SIMPLIFY SUB MATRIX

EF

	A	B	C	D
3	1	0	0	1
4	0	0	0	1
11	1	1	1	0

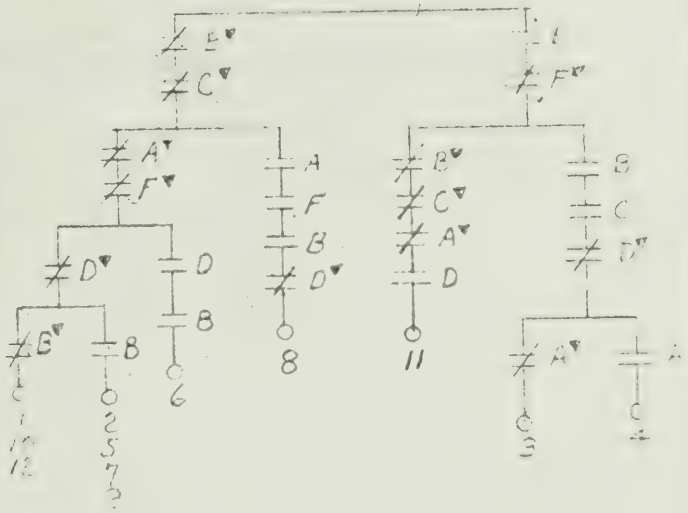
BC

	A	D
3	1	1
4	0	1

B'C'

	D
11	0

STEP IV DRAW RELAY TREE



EQUATION OF SYSTEM

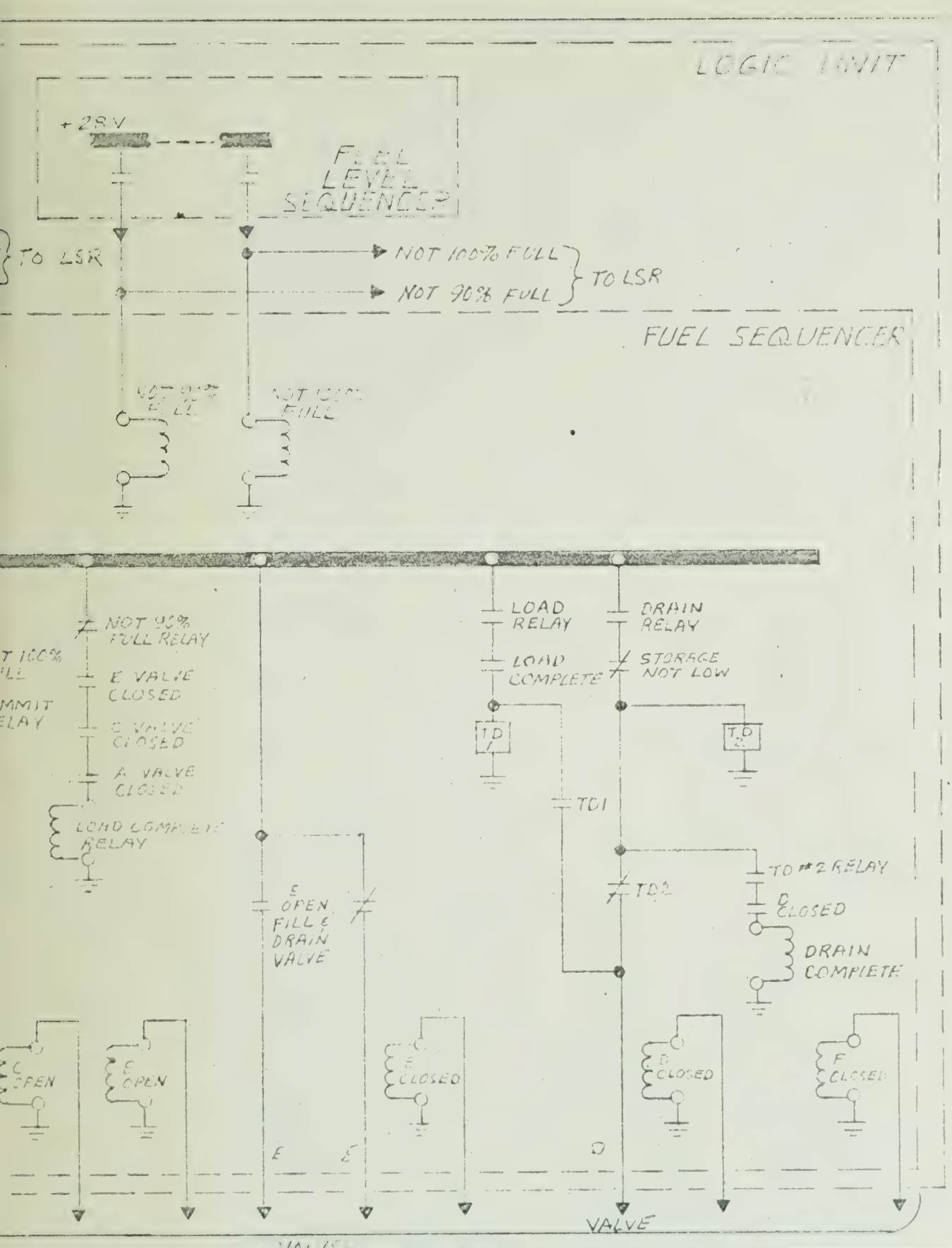
$$F'(D' + BD' + BD) + AF(BD') + EF'\{BCD'(A' + A) + B'C'A'D' + B'C'(E' + E) + BD\} + AFBD' + EF'\{BCD'(A' + A) + B'C'A'D\}$$

1 2 6 8 3 4 11

1 2 11 12 5 7 9

HALLAMORE ELECTRONICS CO.
714 NORTH BROOKHURST ST.
ANAHEIM, CALIF.

TYPICAL EXAMPLE
L.S.R. SUBSYSTEM
DESIGN
SHEET 1 OF 4
DESIGN EXAMPLE



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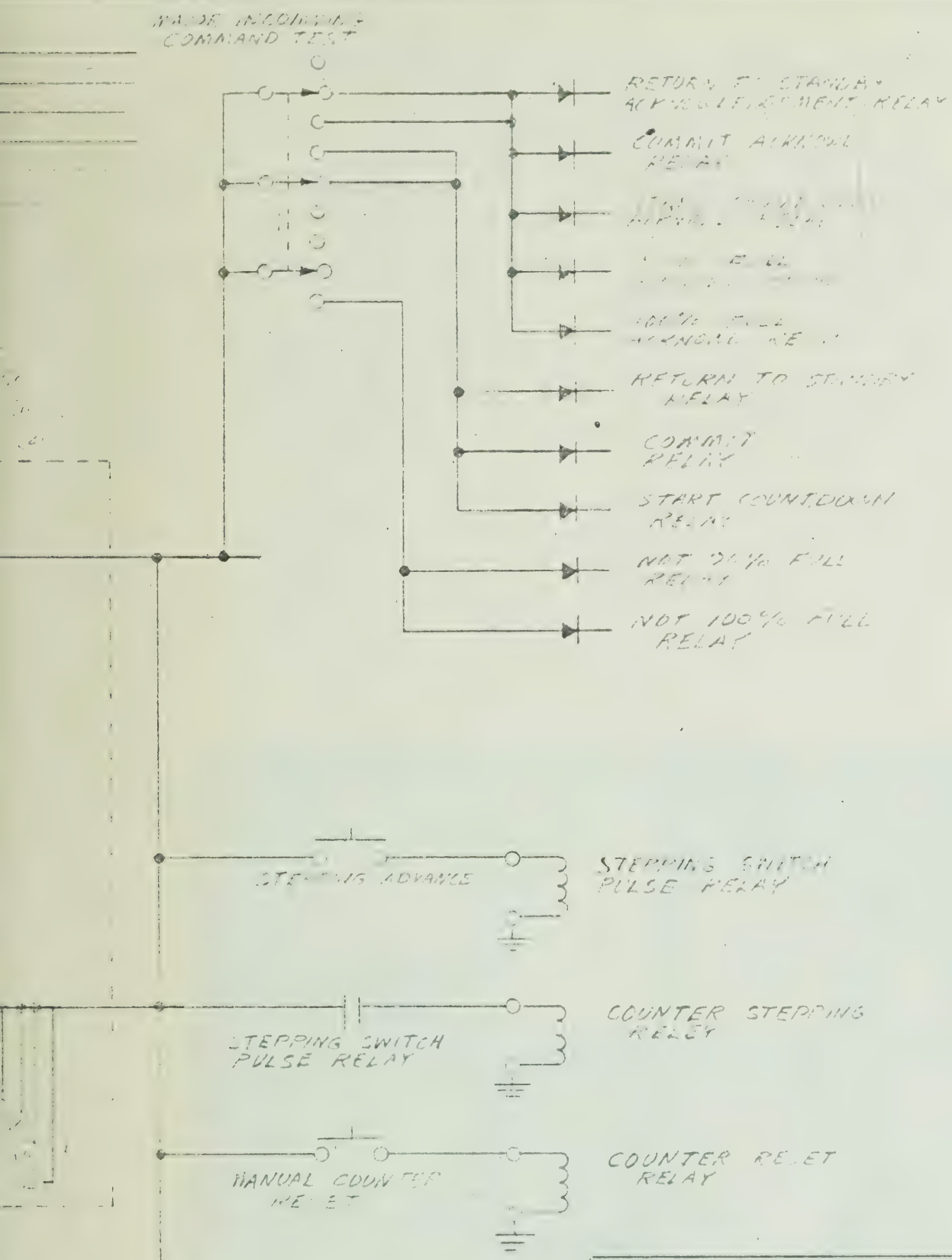
SCHEMATIC - SUB SYSTEM
SEQUENCER

SHEET 2 OF 4
DESIGN EXAMPLE



HALLAMORE ELECTRONICS CO.
714 NORTH BROOKHURST ST.
ANAHEIM, CALIF.

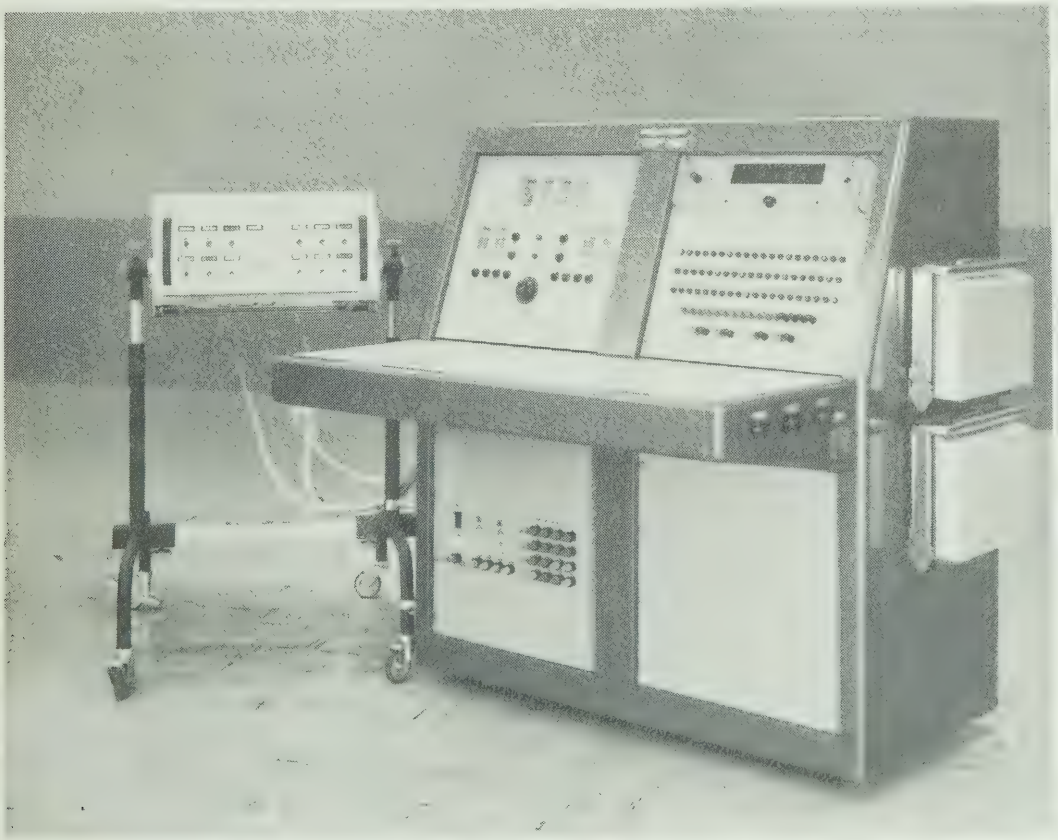
SCHEMATIC
SUBSYSTEM
DESIGN

UNIVERSAL CHASSIS ANALYZER
Model HE-0514

Now available, the Hallamore Universal Chassis Analyzer represents a unique, self-contained test tool designed to supply all required conditioning stimuli and to dynamically checkout complex relay logic circuitry --- in minutes!

Featuring ultra-simple, semi-automatic operation, this Analyzer offers practically unlimited testing capabilities. All stimuli, responses and/or special conditioning signals, etc., are pre-programmed on two easily removable 1632 pin program boards. Programming may be changed at any time to conform to new circuit configurations. Test results are presented by 60 pairs of color coded (green and amber) indicator lamps. Actual conditions of circuits under test are immediately revealed by observing which of the paired lamps are illuminated; both lamps indicate satisfactory operation, the green lamp only indicates lack of desired response, the amber lamp only shows that an unwanted response exists.

The Analyzer will simultaneously monitor up to 60 response points during each of its 47 progressive test steps. Up to 312 individual connections may be made to the circuit under test. Moreover, the Analyzer incorporates additional readout devices for displaying test step number and special operator instructions. An integral interval timer indicates elapsed test time permitting precise time delay measurements. Provisions are also provided for connecting special test equipments as well as applying special stimuli to the Analyzer as required.



CON 105

FUNCTIONAL SPECIFICATIONS:

— The double desk console plus the chassis holding fixture simplifies testing.

— Four 78 pin connectors provide 312 possible connections to chassis for testing.

— All stimuli, responses, special conditioning, fixtures, loads, etc. may be pre-programmed on two removable 1632 pin program boards.

— Analyzer capacity provides 47 separate test steps per set of program boards, plus the following functions for each test step:

a. Thirty isolated DC stimuli circuits

b. Three 400 cycle AC stimuli (AØ, BØ, and CØ)

c. Two pair each of AC and DC monitoring lines.

d. Two of ten possible special instructions.

e. One time delay reference (four digit).

f. Nine switching wafers for programming special stimuli or conditions.

g. Time delay measurement (0.01 millisecond to 9999 seconds in 6 decade steps).

h. Twelve test points.

i. Four Momentary ON switches (momentary circuit closure).

j. Four Momentary OFF switches (momentary circuit interruption).

k. Four 2PDT relays (all terminals available on program board for special tests.

l. Four 2PDT relays (energized during test step to lock in circuitry during test advance of analyzer).

— Immediate observation of test status; 60 pair of green and amber reference and response indicators simultaneously monitor:

a. 45 points of +28 VDC

b. 10 points of -28 VDC

c. 5 points of 115 VAC or 115 VDC (or +28 VDC)

HED UNIVERSAL CHASSIS ANALYZER

(Part #107843)

GENERAL:

The test set is designed as a semi-automatic device with special emphasis on simplicity, reliability, ease of maintenance and requiring minimum skilled personnel for operation. The test set is universal in that it will accept any chassis for test simply by placing the proper pre-programmed patchboards in place and connecting the chassis to the Analyzer by means of test adapter cables.

Test results are presented as an array of lamp indicators where paired sets of indicators represent anticipated response (green) and actual response (amber). A pattern which presents unmatched indicators during test is cause for rejection of the chassis.

Most chassis of the Silo Launch Control equipment will require approximately 15 minutes, plus time delay checks for complete analysis.

FEATURES

1. All programming of stimuli, responses, special conditioning, fixtures, loads, etc. are programmed completely via two 1632 pin program boards.

2. Double desk console w/chassis holding fixture.
   (a) Four 78 pin connectors provide 312 possible connections to chassis for testing.

   (b) Adapter cables of three configuration provide connection to all 70 Silo Launch Control Chassis.

3. Analyzer capacity to provide forty-seven separate test steps per set of program boards and to provide per test step:
   (a) Ten (10) isolated D.C. stimuli circuits. (May be expanded to thirty (30) stimuli)

3. (b) Three (3) 400 cycle AC stimuli (AØ, BØ, & CØ).
   (c) Two pair (2) DC monitoring lines.
   (d) Two pair (2) AC monitoring lines.
   (e) Two (2) of ten special instructions.
   (f) One time delay reference (four digit).
   (g) Nine (9) switching wafers for programming special stimuli or conditions.
   (h) Time delay measurement (.01 millisecond to 9999 seconds).
   (i) Twelve (12) test points.
   (j) Four (4) Momentary ON switch (momentary circuit closure).
   (k) Four (4) Momentary OFF switches (momentary circuit interruption).
   (l) Four (4) 2 PDT relays - all terminals available on program board for special tests.
   (m) Four (4) 2 PDT relays - energized during test step to lock in chassis circuitry during test advance of analyzer.

4. Immediate observation of test status - 60 pair of reference and response indicators (60 green and 60 amber).

BASIC OPERATING PROCEDURE

The chassis is placed in the rotatable holding jig, which is part of the analyzer. The jig permits access to any component or portion of the harness for examination or adjustment during the test. The chassis is connected to the analyzer via adapter cables. The proper program board is inserted in the analyzer but not engaged. Power to the analyzer is turned on, lamp test is conducted, the program board is engaged, and the chassis is ready for test.

The test procedure will define any additional test equipment (scope, multimeters, etc.) required to conduct a complete and valid test on the chassis. Depress "Test Step" button the analyzer control panel to advance test steps. Special instructions to be observed (max. two per test step), are visually presented during test. Test is valid if indicator display presents no unmatched pairs or if specified by test procedure. "End of test" indicated by special instruction indicator.

PROGRAMMING

The Universal Chassis Analyzer provides proper test sequencing by using two 1632 pin program boards, which are inserted in the upper and lower receptacles located on the right side of the console.

Testing may be programmed for simple continuity checks or for complete analysis. Capabilities of the analyzer are such that possible combinations of tests are practically unlimited.

The upper board, designated as Program Board "A", has the primary function of providing stimuli and response signals to the chassis under test. The following programming is accomplished by this board:

Stimuli to chassis under test through P1, P2, P3 & P4
Response from chassis under test to Response Indicators
Test Points
AC & DC metering points
Start & Stop information to interval Counter Power & Returns
Momentary ON switches
Momentary OFF switches
Connection to special conditions receptacle J 11
Connections to Auxiliary 1 & 2 relays
Interconnection to Program Board "B"

The lower board, designated as Program Board "B" has the primary function of providing reference information and special conditions to the analyzer and chassis under test. This includes:

Time delay reference indicator
Response reference indicator
Special Instruction Indicators
Interval Counter Start and Stop Polarity
Interval Counter Range
Auxiliary decks on test stepper switch
Auxiliary Relays 3 thru 6
Auxiliary Fuses 1 thru 3
Interconnection to Program Board "A"

ADVANTAGES OF UNIVERSAL CHASSIS ANALYZER

The method of testing incorporated in this analyzer is the result of considerable research into existing systems, automatic and semi-automatic now available. Surveys of existing systems revealed that no system available at this time could provide the testing of these chassis to the degree and extent necessary to verify their proper operation.

One of the available testing systems considered was the DIT-MCO Model 750 E2M Electro-Mechanical Analyzer. This unit is a universal type, automatic checkout system, capable of actuating relays and resistive devices, providing termination to termination of each circuit for continuity and discontinuity.

The DIT-MCO system was considered for testing of the Silo Launch Control System but rejected because of the following reasons:

1. Inadequate short testing
2. Inadequate time delay measurement capabilities
3. Complexity of the procedure
4. Inadequate trouble-shooting information

Before elaborating upon these points and reviewing the comparison with the Hallamore Universal Chassis Analyzer, the following problems involved in the testing of the Silo Launch Control System Chassis should be considered:

1. Approximately 90% of the testing is of complex relay logic circuitry. The stimuli requirement are: a maximum of ten (10) +28 VDC stimuli per test step, three (3) 115 VAC 400 cycle stimuli per test step and various miscellaneous stimuli.

2. Response measurements require the monitoring of (1) +28 VDC, (2) -28 VDC, (3) 115 VAC and (4) various miscellaneous responses. The maximum number of responses to be monitored are approximately fifty fixed responses and ten miscellaneous responses requiring voltage, resistance, current, etc. measurement.

3. Testing of sensors, amplifiers, servos, meter relays, transducers, etc. require voltage measurements, termination, stimuli, and miscellaneous conditions. This portion of the test sequence consistutes approximately 10% of the test procedure and requires a very flexible method of test programming so as to encompass all test requirements.

4. Measurement of time delays must be made and monitored. Operating intervals of the time delay relays used in the Launch Control chassis range from 0.05 seconds to 7200 seconds. These relays are distributed throughout 80% of the chassis and require measurement and adjustment to an accuracy of $\pm$ 5%.

A comparison study made of the Hallamore Universal Chassis Analyzer Model 107843 and the DIT-MCO Model 250 F2M Electro-Mechanical Analyzer reveal the following differences in operating capabilities:

1. (a) The Hallamore Universal Chassis Analyzer provides ten (10) isolated +28 VDC stimuli per test step (may be expanded to (30) thirty, with complete isolation between inputs to the chassis and any other point within the chassis. It also provides three (3) 115 VAC 400 cycle stimuli (AO, BO, & CO). In addition, nine (9) auxiliary stimuli may be supplied from any external source for programming, through the auxiliary wafers on the test stepper switch.

   (b) The DIT-MCO Analyzer provides for seven (7) +28 VDC or 115 VAC 60 cycle stimuli per test step. It also has the ability of programming (5) externally supplied stimuli.

The testing requirements of a number of the chassis, especially in the responder group require the functioning of relay trees that contain as many as fifteen separate relays. This condition requires fifteen separate stimuli to actuate and test this type of relay logic circuit.

The testing procedure used by Hallamore to verify this type of circuit is to actuate each relay independently to prove the relay is wired correctly. For example the circuit

$$K1 \cdot K2 \cdot \overline{K3} \cdot K4 = 1 \text{ (1 being continuity)}$$

would be tested as follows:

Test 1 $\overline{K1} \cdot K2 \cdot \overline{K3} \cdot K4 = 0$ (0 being discontinuity)

" 2 $K1 \cdot \overline{K2} \cdot \overline{K3} \cdot K4 = 0$

" 3 $K1 \cdot K2 \cdot K3 \cdot K4 = 0$

" 4 $K1 \cdot K2 \cdot \overline{K3} \cdot \overline{K4} = 0$

" 5 $K1 \cdot K2 \cdot K3 \cdot K4 = 1$

This method is used throughout the entire testing procedure to guarantee to the highest degree possible that the chassis being tested is functionally correct.

2. (a) The Hallamore Universal Chassis Analyzer will continuously monitor 60 response points:

45 points of +28 VDC
10 points of -28 VDC
5 points of +28 VDC or 115 V(AC or DC)

In addition to visual display to indicate response points being monitored, reference indicators are also provided, to indicate required response or responses per each test step.
Test points for two AC voltages, two DC voltage measurements per test step, and twelve (12) other test points for measurement and indication are provided.

(b) The DIT-MCO Analyzer provides termination to termination (one per test step) continuity and discontinuity test. It monitors one point per test step, with the last four columns being capable of short testing. (32 test steps).

During the initial phase of the survey and study to determine the testing requirements required to test the Silo Launch Control chassis it was established that due to the complexity of the relay logic circuitry that single point continuity - discontinuity testing would not verify the chassis to the degree required. Nor would the static short testing methods prove that shorts did not exist except in a very few cases.

The results of the study on the chassis indicated that dynamic short testing would be the only method of verifying the chassis to the extent we required. To accomplish this requires the monitoring of all response points, and to determine when the responses are correct or incorrect for any particular test. It was with this thought that the Hallamore Universal Chassis Analyzer was designed.

The DIT-MCO Analyzer in this respect does not verify the chassis to a degree that would satisfy our testing requirements. To program any short testing of a minimum requirement would be difficult and this fact is recognized by the lack of any short testing in the previous chassis that have been programmed for test, by the DIT-MCO Analyzer.

3. (a) The Hallamore Universal Chassis Analyzer provides twelve (12) test points and a special conditions receptacle J11 for the insertion of special stimuli, or for measurement.

   (b) The DIT-MCO Analyzer provides a receptacle for the insertion or external measurement.

4. (a) The Hallamore Universal Chassis Analyzer contains an electronic Interval Counter for time delay measurement. The Interval Counter is entirely programmed through the program boards as to, range, start & stop inputs, start & stop slope (+ or -) and reset. Readout is by means of in-line numerical nixie tubes. Specifications are as follows:

   Maximum Count - 9999 (4 digit) seconds.
   Ranges - 0.01 MS, D.1 MS, 1.0 MS, 0.01 Sec., 0.1 sec., 1 sec.
   Accuracy - 0.005% ± 1 clock pulse
   Input Sensivity - 1 Volt DC coupled
   Impedance - 1 Meg. shunted by 50 MMF

   (b) The DIT-MCO Analyzer contains an electro-mechanical timer, which has the following specification:

   Range - Totalizing 60 minutes
   Scale Dev. 0.01 sec.
   Accuracy 0.002% per division ± 1 division

The chassis of the Silo Ground Control System contain time delay relays with delay ranging from 0.05 sec. to 7200 seconds. Both time delay dropout and time delay pullup relays are used and must be checked and set to a tolerance of ± 5%.

To set the 0.05 second time delays which are used to a great extent in the responder group of chassis, it is necessary to have a counter that has a readout of 0.001 seconds. The tolerance of 0.05 second ± 5% is 475 millisecond to 525 millisecond.

Using the counter employed in the DIT-MCO analyzer it is only possible to set this time delay ± 30% (minimum division plus counter accuracy).

The counter employed in the Hallamore Chassis Analyzer is capable of setting the time delays to an accuracy of 0.005% if desired.

Another advantage of the electronic counter over the mechanical timer used by DIT-MCO is in the measurement of TDDO (Time delay dropout) relays. The electronic counter may be started and stopped by either a positive or negative going pulse, whereas, the electro-mechanical counter requires a +28 VDC voltage to operate the counter. In many cases it is not possible to obtain this signal directly from the chassis under test.

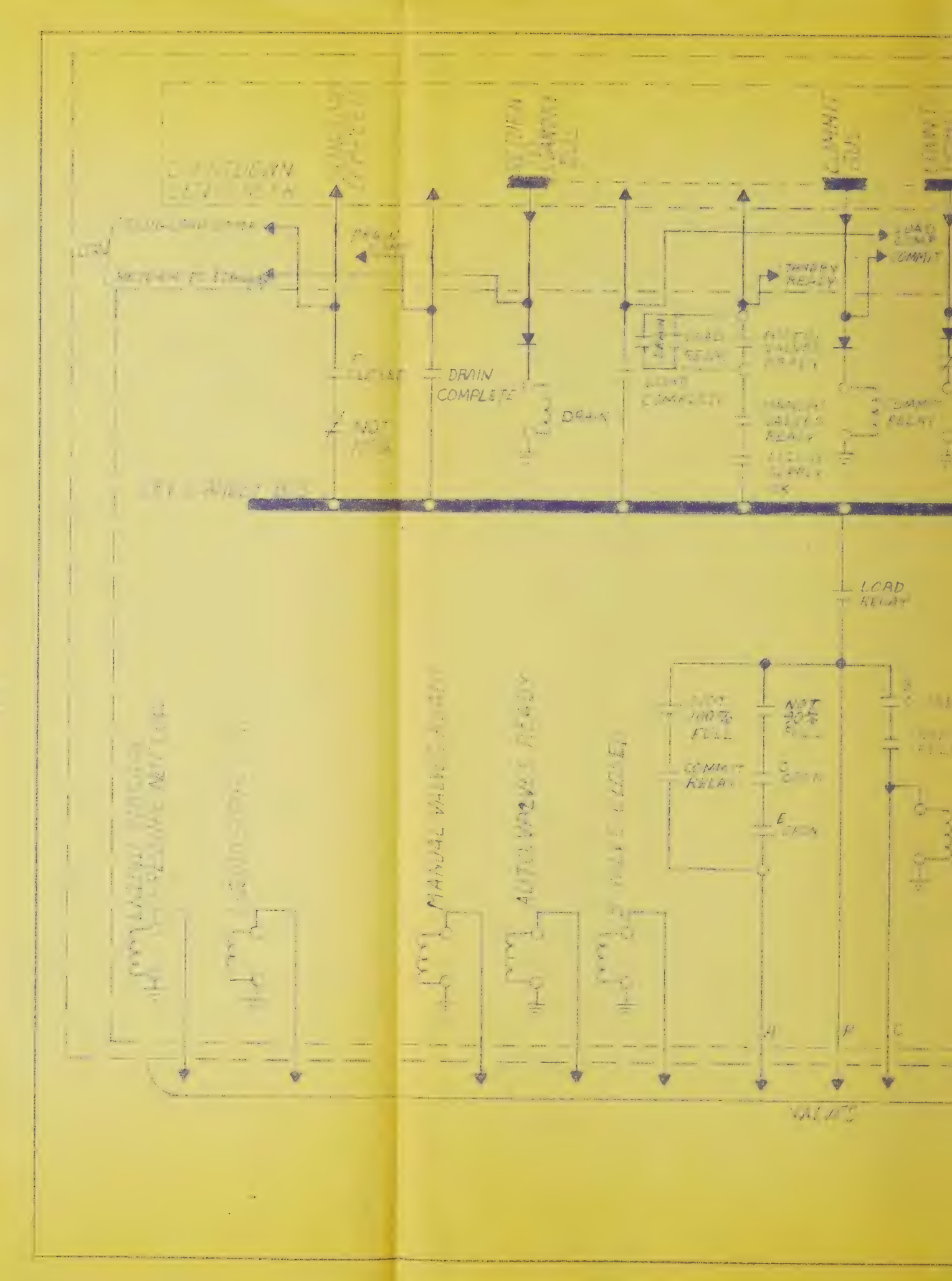
SUMMARY

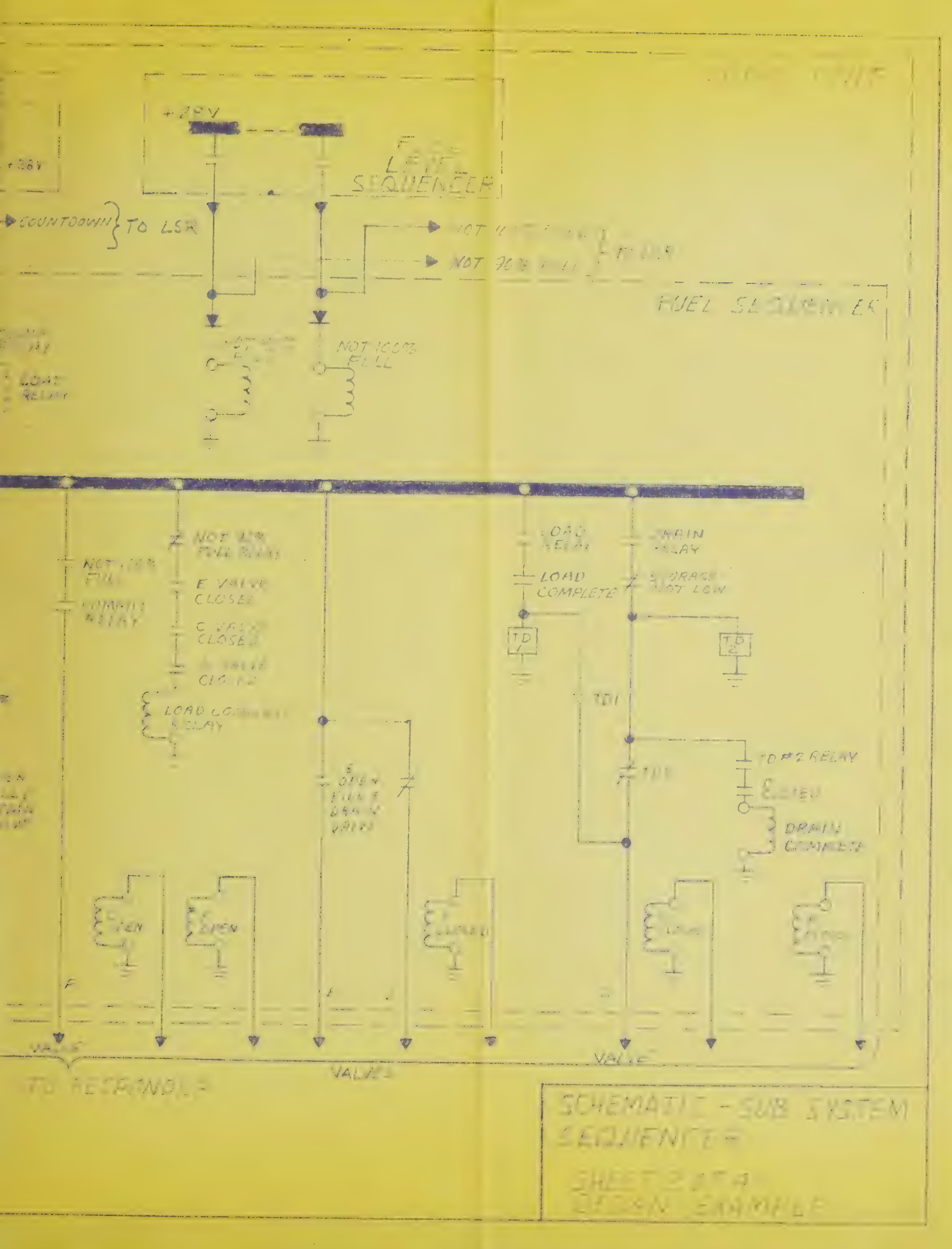
In addition to the advantages outlined above of the Hallamore Universal Chassis Analyzer, a greater advantage is to be gained in cost savings of programming and modification to programming of the Analyzer in the field. The Hallamore Electronics Division at present is using the Universal Chassis Analyzer for in-plant production checkout of the Silo Launch Control

chassis and has all programming and procedures completed for this task. It has been estimated that programming for the DIT-MCO Analyzer requires approximately 100 hours per chassis, this is roughly 7,000 hours of engineering time completed by HED at this time.

In addition, modification of chassis in the field requires a modified Testing Procedure and modified programming for the DIT-MCO Analyzer. This modification is automatically accomplished for the production chassis at HED and could be supplied as part of the modification kit when shipped to the field.

Although the present model of the Universal Chassis Analyzer is basically of commercial design and uses commercial grade of components, the proven basic design is readily adaptable to ruggedized field version. Its design will also allow for additional metering (voltage, resistance, current) to be incorporated in the display section.


DRAIN
COMPLETE
DRAIN
LOAD
RELAY
COMMIT
TIMER
RELAY
LOAD
RELAY
NOT
20%
FULL
COMMIT
RELAY
MANUAL
AUTOMATIC
A
B
C


+28V
SEQUENCER
COUNTDOWN
TO LSR
NOT 100% FULL
FUEL SEQUENCER
LOAD RELAY
NOT 100% FULL
NOT 100% FULL
E VALVE CLOSED
C VALVE CLOSED
LOAD COMPLETE RELAY
LOAD RELAY
DRAIN RELAY
LOAD COMPLETE
STORAGE NOT LOW
TD 1
TD 2
TD1
TD #2 RELAY
TD1
DRAIN CONTACT
E OPEN
E OPEN
VALVE
VALVES
VALVE
TO RECEIVER
SCHEMATIC - SUB SYSTEM SEQUENCE
SHEET 2 OF 4
OPEN EXAMPLE

SIGNAL RESPONSE
CRITERIA FOR
DESIGN CRITERIA

INDEX

1.0 INTRODUCTION

1.1 Scope and Purpose

This design criteria is written to define and establish the basic design philosophy of the Launch Signal Responder. (LSR).

This design criteria will outline and define the complete design task of the LSR based on the premise of minimum change in the presently designed Launch Control System.

A general example outlines a complete step by step design of a typical LSR subsystem. For better understanding of the interface problem between the sequencer subsystem and the LSR Subsystem the Logic Unit Sequencer design is included in the design example.

1.1.1 Overall System Description

The LSR in the Responder mode will exercise the Launch Control System in real time, and isolate malfunctions to a particular subsystem in the Logic Unit. The LSR will also have an automatic test capability on the subsystem level.

2.0 GENERAL DESCRIPTION OF LSR

2.1 Basic Design Concept

The basic design concept of the LSR is based on checking that the output of the Logic Unit Sequencers corresponds to a definite pre-established operational sequence of the end components which are controlled by the Logic Unit Sequencers.

This is accomplished by checking the outputs of the sequencers to a pre-established fixed control matrix.

The interface signals between subsystem sequencers will be checked with respect to their relative position in the sequence.

The process of a definite operational sequence of the end components is simulated in the LSR.

Monitoring of the simulated process in the LSR will establish the physical relationship between the various subsystems.

Checking the intermediate steps of the process in the LSR with the acknowledgments received from the sequencers determines whether the sequencer responses are true or false.

3.0 DEFINITIONS FOR DESIGN PHILOSOPHY AND CRITERIA

3.1 Definitions

In order to establish a uniform design for the LSR the terms used in the design philosophy are defined below:

3.1.1 Definition of Command

Command is defined as a control signal which will initiate a change in the sequence of operation.

3.1.1.2 Definition of Major Command

A major command is defined as an interface signal between sequencers.

3.1.1.2.1 Definition of Major Incoming Command

A major incoming command is defined as a control signal received by the sequencer to initiate a logic sequence in the subsystem.

3.1.1.2.2 Definition of Major Outgoing Command

A major outgoing command is defined as a control signal sent by the sequencer to start a logic sequence in the subsystem receiving the signal.

3.1.1.3 Display of Commands

3.1.1.3.1 Major Incoming Command Display

All major incoming commands will be displayed on the LSR subsystem panel by a green light.

3.1.1.3.2 Display of Major Outgoing Commands

No major outgoing command will be individually displayed on the LSR - subsystem panel.

If an outgoing command does not appear or is out of sequence the LSR subsystem status light will indicate a red condition and the LSR sequence will stop.

3.1.1.3.2 Display of Major Outgoing Commands - cont.

For general conditions circuit will be as in design example. If an outgoing command does not appear in the tree a priority check on the incoming command is made.

3.1.1.4 Definition of Minor Command

A minor command is defined as a control signal to any end component in the missile or GSE for any phase of operation.

3.1.1.5 Minor Command Display

No individual minor commands will be displayed on the LSR Subsystem panel. Indication in form of a numerical display will be provided to indicate the number of a minor command being generated by the Logic Unit Sequencer.

If a minor command does not appear or is out of sequence the LSR Subsystem Status Light will indicate a malfunction.

When a Subsystem sequence is completed satisfactorily the LSR Subsystem Status Light will become Green, indicating satisfactorily Subsystem operation.

3.2 System for Matrix Representation

The following conditions are established to standardize a system design.

3.2.1 Valve Command Representation

3.2.1.1 Motor Operated Valves

The motor operated valve will be represented by a latching relay consisting of Coil A and Coil B.

In Valve Matrix (Open Valve Position = 1
(Closed Valve Position = 0

In Relay Matrix (Energized Contact of Coil A = X
(Energized Contact of Coil B = X'

X' = 0 X = 0

3.2.1.2 Pneumatic or Solenoid Operated Valves

The pneumatic or solenoid operated valves will be represented by a normal relay.

In Valve Matrix (Open Valve = 1
(Closed Valve = 0

In Relay Matrix (Energized Relay Contact = Y
(Deenergized Relay Contact = Y'

then in relay matrix Y = 1
Y' = 0

Note: For normally closed valves valve matrix terms equal relay matrix terms. For normally open valves the valve matrix terms are opposite to the relay matrix terms.

3.2.2 End Components Representation

Accomplishment of a positive action which requires application of power such as activate battery, missile loads on, etc., will be designated as 1.

Reverse condition as 0.

3.3 Fault Insertion

General Fault Insertion -

The Faults are inserted in the feedback or replay circuit of the end components or in the control circuitry depending on individual case.

3.3.1 Individual Fault Insertion

a. For end components there will be limited Fault Insertion.

b. Major Incoming Commands partial Fault Insertion.

(Command failed to appear)

c. Major Process Parameters.

d. Partial Fault Insertion.

3.4 Design Philosophy

For the proper operation of the LSR a specific procedure has to be followed prior to exercising the Launch Control System in the Responder mode. The same procedure has to be followed in case a malfunction has appeared in one or more sequencers during the Responder Mode.

3.4.1 Resetting the LSR

Resumption of Launch Control System checkout through the LSR after an occurrence of a malfunction will be accomplished as follows:

a. All power is shut off in each Logic Unit Sequencer.

b. All power is shut off in each LSR Subsystem.

Upon replacement of faulty sequencer in the Logic Unit power is turned on in the LSR and Logic Units. When no malfunction occurs and standby condition is established for all Logic Unit Sequencers a responder countdown and check is initiated.

3.4.2 Major Commands in Series Interface Between Sequencers.

When there is a series chain of outgoing major commands in various Logic Unit Sequencers a special arrangement is made in each Logic Unit Sequencer

Two possibilities exist to achieve the desired results. They are presented in order of simplicity.

a. Arrange contacts in sequential order versus time. 28 V is applied at the first command.

b. Insertion of an isolation relay in the sequencers which are in the middle position of the series string.

c. Isolation between Logic Unit Sequencers will be accomplished by inserting a diode at the receiving Logic Unit subsystem.

Note: See design example sequencer sketch.

3.4.2 Major Commands in Series Interface Between Sequencers

d. Any major incoming command which forms a series string through the Logic Unit sequencer will not be displayed on the LSR subsystem panel.

Note: Diode isolation will be provided in the receiving logic unit subsystem. A relay in the LSR will indicate the presence or absence of the above defined command.

4.0 TYPICAL DESIGN EXAMPLE

4.1 Description of Physical Process

The objective is to load the upper tank with fluid in two phases of operation.

Upon load completion a line drain is desired.

Valve matrix in effect Fig. will explain the process completely.

4.1.1 Problem

The problem consists of designing an LSR to the existing sequencer that will fulfill the requirements outlined in this criteria.

5.0 LSR SUBSYSTEM TEST

5.1 LSR Subsystem Test Criteria

The LSR subsystem test is performed to obtain assurance that the LSR subsystem indicating a malfunction in the Logic Unit sequencer is functioning properly.

5.1.1 Design Philosophy of the LSR Subsystem Test

The design objective of the LSR subsystem test is to determine in minimum time the integrity of the LSR sequence. This is accomplished by simulating all incoming and outgoing signals into the LSR subsystem.

5.1.2 LSR Subsystem Test Procedure

The LSR subsystem test is performed as follows:

a. Panel power is shut off in the corresponding Logic Unit subsystem.

b. LSR load test is placed in test position.

5.1.2.1 Major Incoming Command Test

a. Set responder switch at launch mode and unplug the LSR plugs at the umbilical junction box.

b. Major incoming command test switch is placed in test position and all major incoming command lights will illuminate (green). Nondisplayed major incoming command test light will illuminate (green).

5.1.2.2 LSR Subsystem Sequence Test

The LSR subsystem sequence test will be performed by a stepping switch. The stepping switch will be advanced manually and a visual comparison between two counters is made by the operator. Corresponding numbers on the numerical displays will indicate a "Go" condition and then the next step shall be performed.

5.0 SUMMARY

This design criteria and circuitry developed in the example LSR design will be used throughout the design of the LSR for the existing Launch Control System of EOC concept.

III SOLVING OF RELAY MATRIX

a. REDUCE THE MATRIX BY REMOVING ROWS IN WHICH CONTACTS ARE DUPLICATED

	A	B	C	D	E	F
	1	1	1	1	1	1
	1	0	1	1	1	1
3	1	0	0	1	0	1
4	0	0	0	1	0	1
6	1	0	1	0	1	1
8	0	0	1	1	1	0
11	1	1	1	1	0	0
1	5	2	5	5	4	6
0	2	5	2	2	3	1

OPTIMIZE FOR MINIMUM CONTACT COMBINATION TAKE OUT E

DEVELOPE SUB MATRIX OVER B COLUMN

E:

	A	B	C	D	F
3	1	0	0	1	1
4	0	0	0	1	1
11	1	1	1	0	1

SIMPLIFY SUBMATRIX

EF

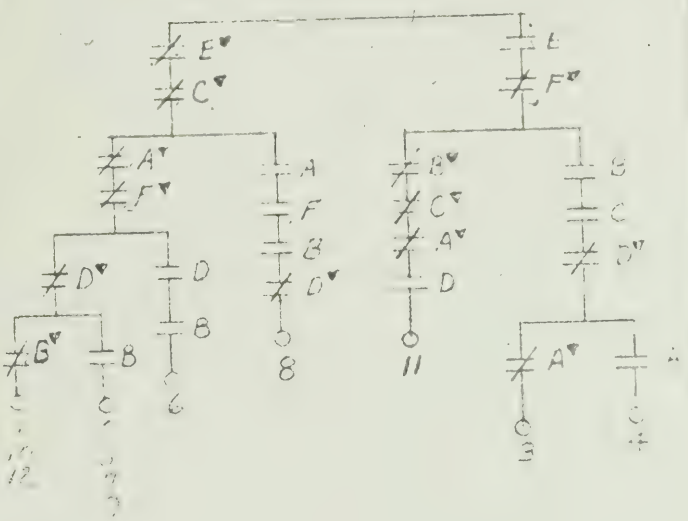
	A	B	C	D
3	1	0	0	1
4	0	0	0	1
11	1	1	1	0

BC

	A	D
3	1	1
4	0	1

STEP IV

DRAW RELAY TREE



OF SYSTEM.

$+ BD' + BD) + AF(BD')\} + EF'\{BCD'(A' + A) + B'C'A'D'\}$

$B' + B) + BD\} + AFBD'] + EF'\{BCD'(A' + A) + B'C'A'D\}$

1 2 6 8 3 4 11

10 5

12 7

9

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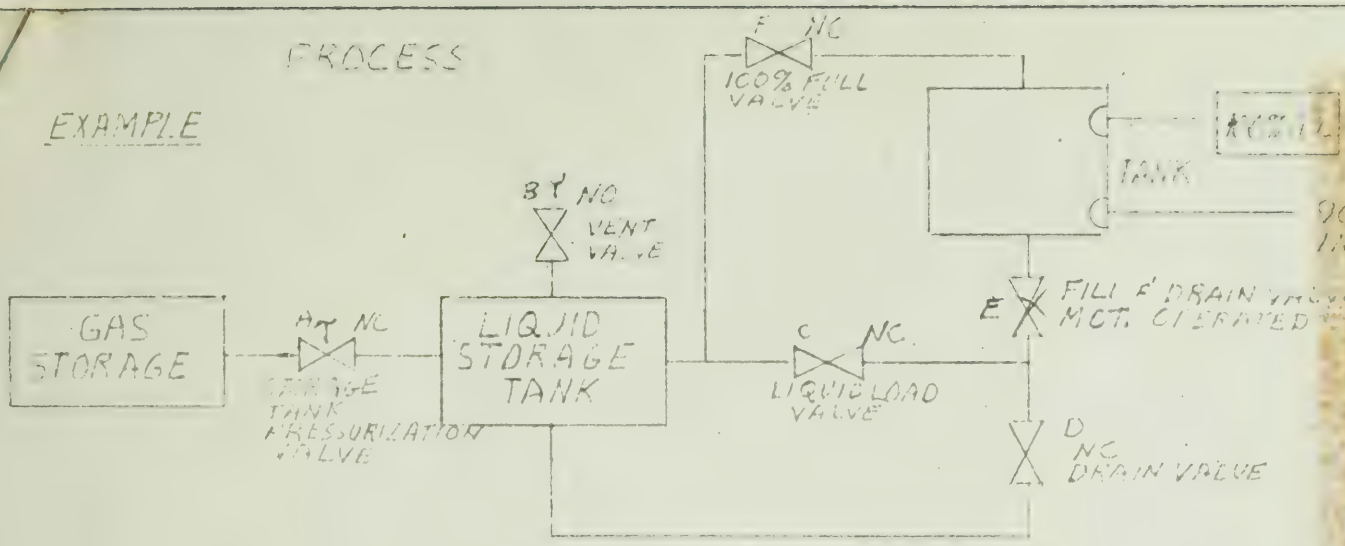
ANAHEIM, CALIF.

TYPICAL EXAMPLE
L.S.R. SUBSYSTEM
DESIGN
SHEET 1 OF 4
DESIGN EXAMPLE

PROCESS

EXAMPLE



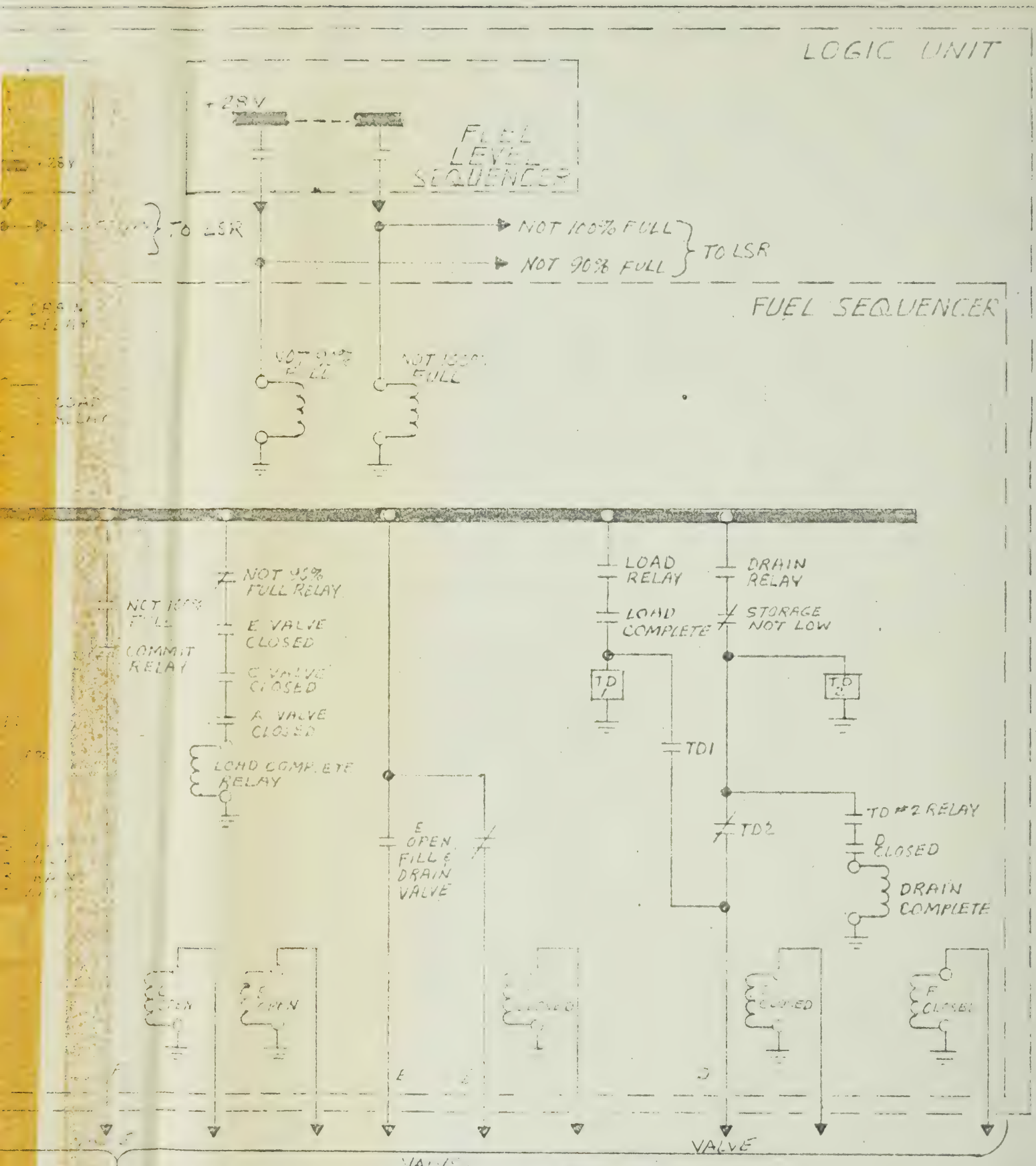
STEP I SETUP VALVE MATRIX

0 = OPEN 1 = CLOSED

		A	B	C	D	E	F
1	MAJOR COMMAND STANDBY	1	0	1	1	1	1
2	MAJ. COM. START COUNTDOWN	1	1	1	1	1	1
3	MIN. COM. START 1	1	1	0	1	0	1
4	MIN. COM. START 2		1	0	1	0	1
5	MAJ. COM. 90% FULL	1			1	1	1
6	MIN. COM. START 3	1	1	1	0	1	1
7	MIN. COM. START 4	1	1	1	1	1	1
8	MAJ. COM. COMMIT		1	1	1	1	0
9	MAJ. COM. 100% FULL	1	1	1	1	1	1
10	MIN. COM. #5	1	1	1	1	1	1
11	RETURN TO STANDBY FROM END OF COUNTDOWN	1	0	1	0	0	1
12	MIN. COM. #6 DRAIN COMPLETE	1	0	1	1	1	1

STEP II DRAW RELAY MATRIX

	A	B	C	D	E	F
1	1	1	1	1	1	1
2	1	0	1	1	1	1
3	1	0	0	1	0	1
4	0	0	0	1	0	1
5	1	0	1	1	1	1
6	1	0	1	0	1	1
7	1	0	1	1	1	1
8	1	0	1	1	1	0
9	1	0	1	1	1	1
10	1	1	1	1	1	1
11	1	1	1	0	0	1
12	1	1	1	1	1	1



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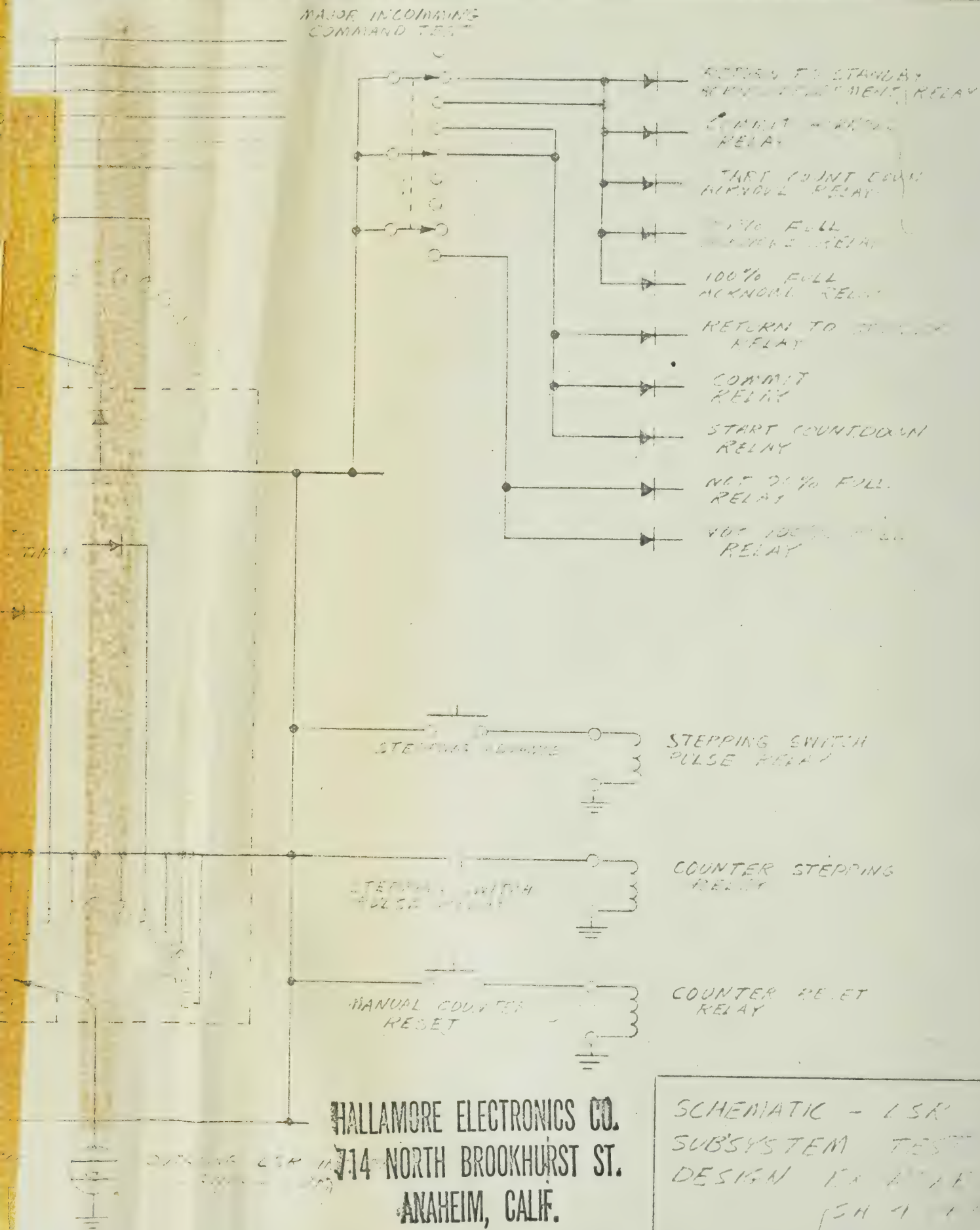
SCHEMATIC - SUB SYSTEM
SEQUENCER

SHEET 2 OF 4
DESIGN EXAMPLE

COUNTDOWN
SLUG LOAD COMP
LSR
MAIN COM
RETURN TO STANDBY
STANDBY READY
DRAIN
COMPLETE
NOT
STANDBY
MANUAL
AUTO
COMMIT READY
LIQUID
LIGHTS



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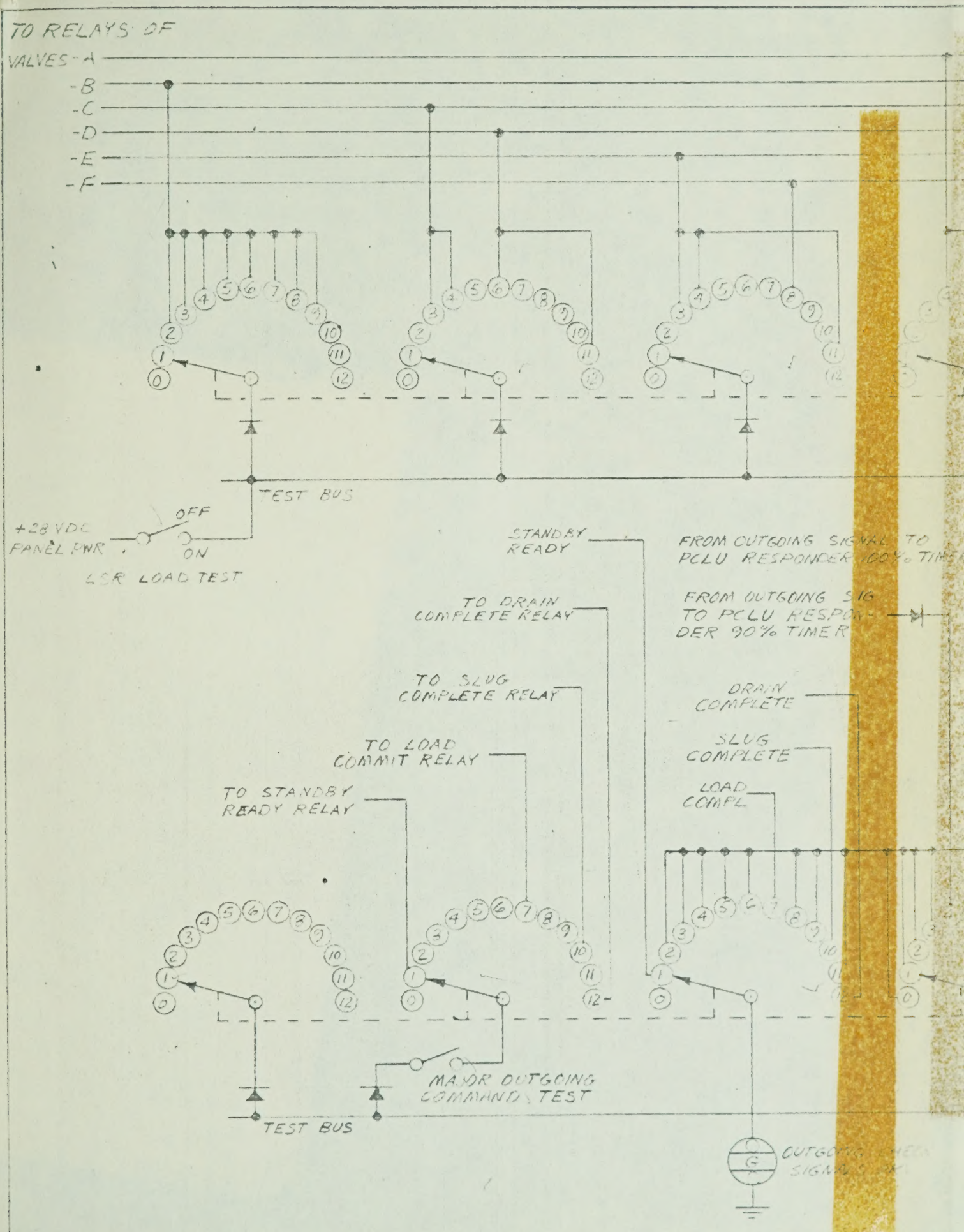
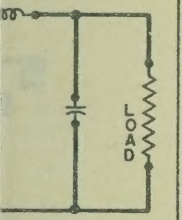
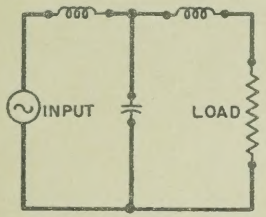
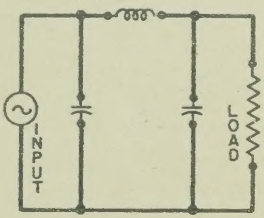
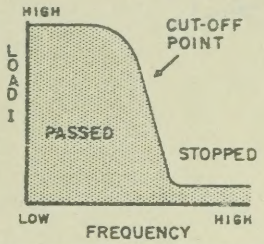
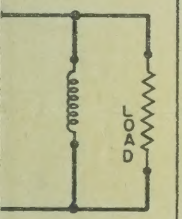
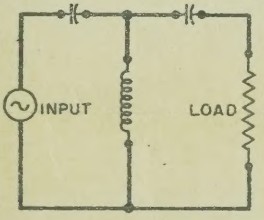
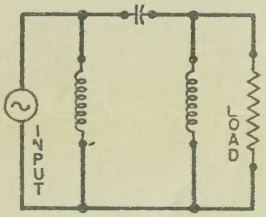
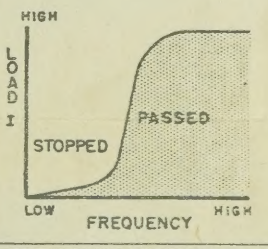
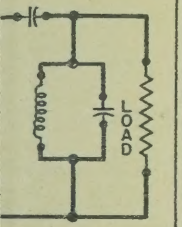
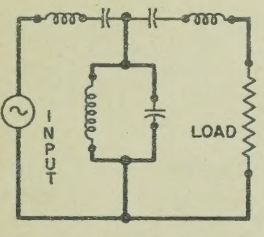
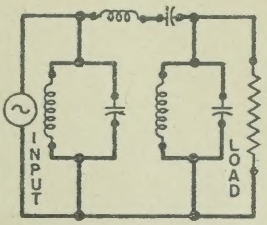
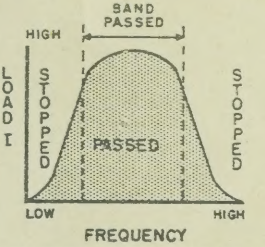
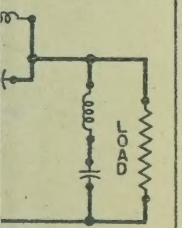
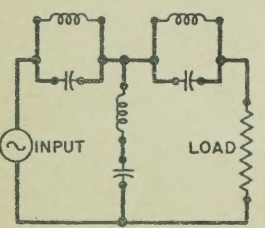
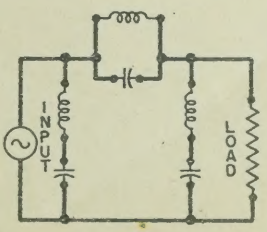
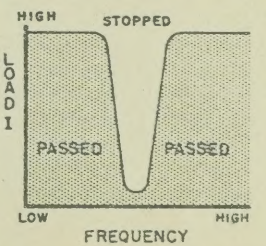
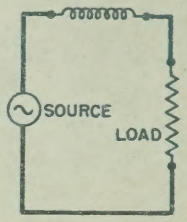
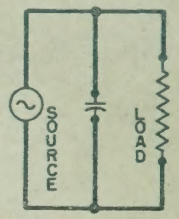
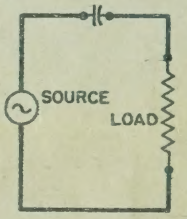
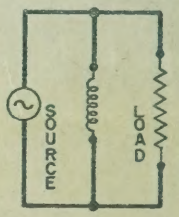
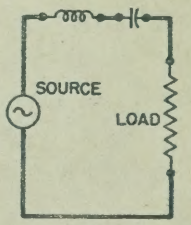
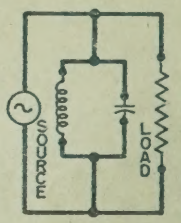
SCHEMATIC - LSR
SUBSYSTEM TEST
DESIGN


TO RELAYS OF VALVES
-A
-B
-C
-D
-E
-F
TEST BUS
+28 VDC PANEL PWR
OFF
ON
LSR LOAD TEST
STANDBY READY
FROM OUTGOING SIGNAL TO PCLU RESPONDER 100% TIME
FROM OUTGOING SIG TO PCLU RESPONDER 90% TIMER
TO DRAIN COMPLETE RELAY
TO SLUG COMPLETE RELAY
TO LOAD COMMIT RELAY
TO STANDBY READY RELAY
DRAIN COMPLETE
SLUG COMPLETE
LOAD COMPL
MAJOR OUTGOING COMMAND TEST
TEST BUS
G

TYPE	"T" TYPE	"π" TYPE	FREQ RESPONSE CHARACTERISTICS
			
			
			
			

TYPE	CONSTRUCTION	SIMPLE	
		SERIES	PARALLEL
LOW-PASS	1. A CAPACITOR IN PARALLEL WITH LOAD. 2. AN INDUCTOR IN SERIES WITH LOAD. 3. ANY COMBINATION OF BOTH.		
HIGH-PASS	1. AN INDUCTOR IN PARALLEL WITH LOAD. 2. A CAPACITOR IN SERIES WITH LOAD. 3. ANY COMBINATION OF BOTH.		
BAND-PASS	1. A PARALLEL TUNED CIRCUIT IN PARALLEL WITH LOAD. 2. A SERIES TUNED CIRCUIT IN SERIES WITH LOAD. 3. ANY COMBINATION OF BOTH.		
BAND-REJECT	1. A SERIES TUNED CIRCUIT IN PARALLEL WITH LOAD. 2. A PARALLEL TUNED CIRCUIT IN SERIES WITH LOAD. 3. ANY COMBINATION OF BOTH.